Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp760-761

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In-Depth Study on Mechanism of the Performance Improvement by High Temperature Annealing of the Al_2O_3 in a Charge-Trap Type Flash Memory Device

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1. Introduction

Charge-trap type memory devices, known as TANOS have attracted attention due to excellent potential to substitute for floating gate-type memory devices [1]. Recently, it has been demonstrated that high temperature oxygen annealing (HTOA) of Al_2O_3 blocking layer can improve the retention property in conjunction with program/erase and endurance characteristics [2]. They concluded that origin of the retention enhancement is due to the reduced trap assisted tunneling (TAT) current through Al_2O_3 blocking layer. However, detail charge loss mechanism has not been investigated. In this paper, we present in-depth study on the mechanism of the performance improvement by HTOA process.

2. Experiments

The n-channel MOS capacitors of 100×100 um^2 with ONA thickness (4.5/6/9,12,15 nm) were fabricated, followed by 1100°C post-deposition annealing (PDA) in a N_2 or O_2 ambient. 150 nm TaN was deposited by reactive sputtering for the gate metal.

3. Results and Discussions

Figure 1 shows the retention property of devices with different PDA conditions. Compared to N_2 PDA, O_2 PDA samples exhibit better retention property, which is coincident with reference [2]. Since the equivalent oxide thickness (EOT) is slightly increased by O_2 PDA, charge loss amount *vs*. gate stack EOT is plotted for better comparision in Fig. 2. The result reveals that O_2 PDA samples still show better retention property even at the same gate stack EOT.

To investigate the mechanism of such an improvement, charge loss amount after 24 hrs baking as a function of bake temperature is measured (Fig. 3). The thinner Al_2O_3 shows more charge loss at 250°C. This indicates that as the thickness of Al_2O_3 is thicker, thermionic emission component (TEC) of the charge loss decreases and in other words, Al_2O_3 conduction band offset against Si_3N_4 trapping layer also increases by high temperature PDA process, which is not coincident that thermionic emission is not sensitive to the blocking thickness [3]. Moreover, in case of 9 nm Al_2O_3 samples, N_2 and O_2 PDA samples show the same trend on changes of charge loss in the range of 25 ~ 250°C. However, in case of 15 nm Al_2O_3 samples, charge loss of O_2 PDA sample is much smaller than that of N_2 PDA samples at 250°C. From this result, we can speculate that O_2 PDA increases Al_2O_3 potential barrier due to enhancement of crystallinity of Al_2O_3, leading to better retention property. Fig. 4 shows the difference of the charge loss amount monitored by the flat-band voltage difference between 150ºC and 250ºC, which indicates the pure TEC. This result also shows that TEC is greatly reduced by HTOA when the gate stack EOT is more than 12 nm. The charge loss amount ΔQ is also extracted from the retention measurement at 85ºC, as shown in Fig. 5. It is known that the leakage mechanism is first caused by the direct tunneling through oxides and then followed by TEC [3]. In our result, TEC is greatly reduced by O_2 PDA process for the cases of gate stack EOT of more than 12 nm. Therefore, at least 12 nm Al_2O_3 blocking layer is needed to effectively suppress TEC by HTOA.

To investigate the changes of conduction band offset of Al_2O_3 by N_2 and O_2 PDA, energy loss spectrum is derived from the O 1s spectrum by XPS (Fig. 6) [4]. The result shows that there is no meaningful difference in the extracted energy band gap between N_2 and O_2 PDA samples ($E_{G,\ Al2O3}$ = 7.5, 7.58 eV for N_2 and O_2 PDA). Instead, the amount of relative trap density as a function of the trap energy level, calculated from charge loss rate, shows that the thicker Al_2O_3 samples have deeper trap energy level (Fig. 7). In other words, if the trapping energy level of all samples in Si_3N_4 layer is similar, the conduction band offset of Al_2O_3 will be higher after N_2 and O_2 PDA. In addition, unlike N_2 PDA, 12 nm Al_2O_3 HTOA sample shows similar trap density profile compared to 15 nm Al_2O_3 HTOA sample.

Trap-assisted-tunneling (TAT) current component was also investigated by monitoring charge loss amount at 25°C after 1 day and 20 days baking, as shown in Fig. 8. There's no significant difference in TAT current after 1day, however, O_2 PDA sample shows larger charge loss than N_2 PDA sample after 20 days, indicating a higher bulk trap density for HTOA sample, which is coincident with reference [6]. TAT current can be also identified by measuring the trapping rate or trapping efficiency (TE) [7]. Fig. 9 shows the change of gate voltage during a constant current stress test performed on TANOS devices and Fig. 10 shows the TE calculated from Fig. 9 [8]. The result reveals that the TE of N_2 PDA samples is smaller than that of O_2 PDA samples, implying that the TAT current through the Al_2O_3 defect in a programmed state can be more suppressed by high temperature N_2 PDA process.

4. Conclusion

Enhanced retention property upon high temperature O_2 PDA can be contributed to not suppressing the TAT current but changes of the conduction band offset of the crystallized Al_2O_3.

Acknowledgements

This work was supported by Hynix Semiconductor Inc., Jusung Engineering Co. and UP Chemical Co..

References

[1] H. T. Lue, et al., ICSICT (2008) 807.
[2] A. Rothschild, et al., ESSDERC (2009) 272.
[3] S.S. Chung, et al., IEDM (2003) 617.
[4] S. Miyazakia, et al.,J. Vac. Sci. Tech.B. 19 (2001) 2212.
[5] Y. Yang, et al., Sol.-State Electon. 44 (2000) 949.
[6] M. Toledano-Luque, et al., IEDM (2009) 749.
[7] S.H. Lee, et al., IEEE Elec. Dev. Lett. 31 (2010) 266.
[8] C. Papadas, et al., J. of Appl. Phys. 71 (1992) 4589.

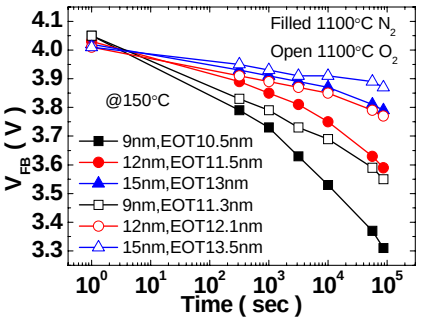

Fig. 1 Retention characteristics of TANOS devices with different PDA conditions.

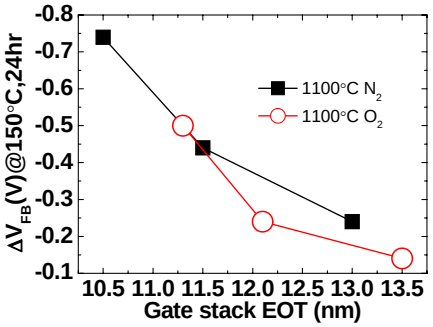

Fig. 2 Charge loss amount of devices with different PDA conditions as a function of gate stack EOT at 150°C after 24 hrs baking.

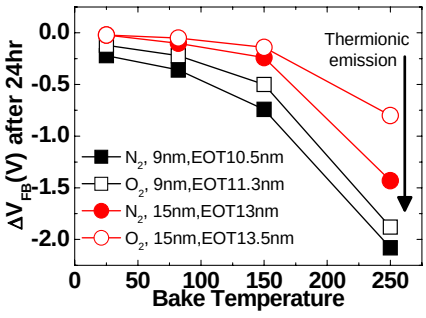

Fig. 3 Charge loss amount of devices with different PDA conditions as a function of baking temperature after 24 hrs baking.

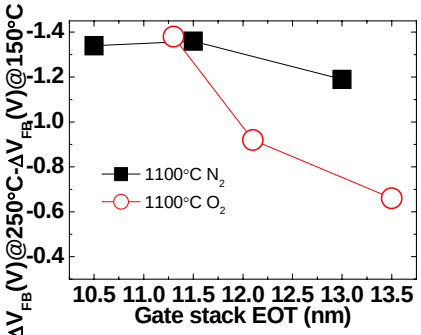

Fig. 4 Flat-band voltage difference between 150°C and 250°C after 24 hrs baking as a function of gate stack EOT.

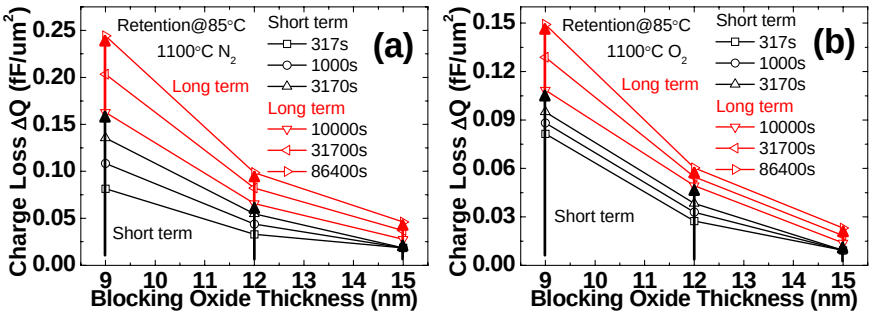

Fig. 5 Charge loss characteristic against different blocking oxide thicknesses for (a) N_2 annealed and (b) O_2 annealed samples. The data are extracted from the retention measurement up to 24 h at 85°C by $\Delta Q = C_{ox} \cdot \Delta V_{FB}$ [3]. Short term charge loss means thickness-dependent tunneling component through Al_2O_3 blocking layer. Long term charge loss means the thermionic emission component [3].

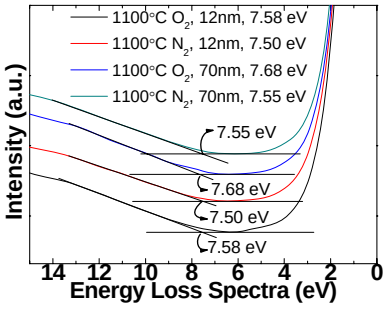

Fig. 6 Energy loss spectrum derived from the O 1s spectrum as measured by XPS to extract the energy bandgap values [4].

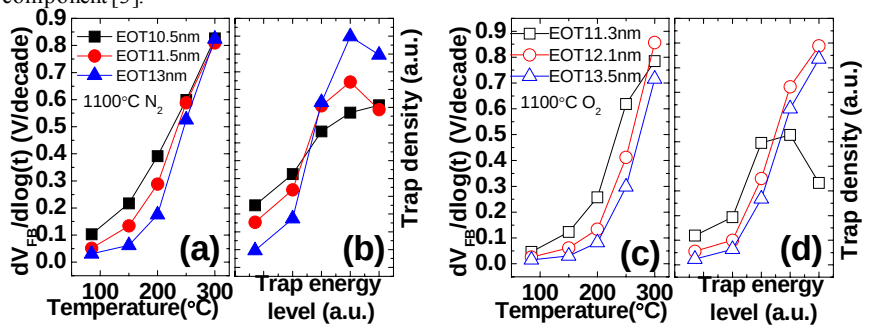

Fig. 7 Charge loss rate of (a) N_2 annealed and (c) O_2 annealed samples as a function of retention measurement temperature. Relative trap density amount of (b) N_2 annealed and (d) O_2 annealed samples as a function of the trap energy level, extracted from Fig. 7(a),(c), respectively [5].

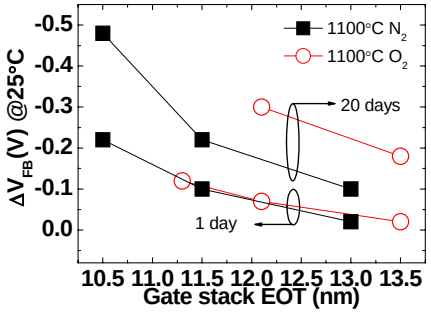

Fig. 8 Charge loss amount of devices with different PDA conditions as a function of gate stack EOT at 25°C after 1day and 20days baking.

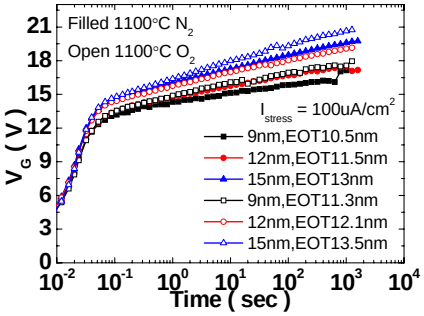

Fig. 9 Change in the gate voltage during a constant current stress test performed on TANOS devices annealed at different PDA conditions.

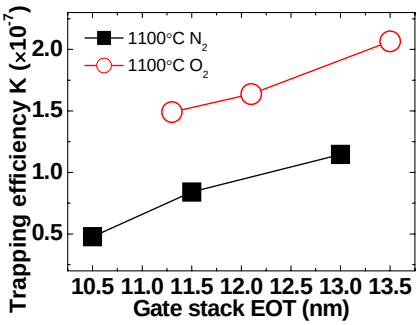

Fig. 10 Trapping efficiency K of devices with different PDA conditions. It is extracted from the figure of trapped charge in Al_2O_3 versus injected charge (not shown), calculated from Fig. 9 [8].