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POST-BREAKDOWN RECOVERABLE METAL NANOCRYSTAL-BASED AL_2O_3/SIO_2 GATE STACK FOR NON-VOLATILE MEMORY

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Abstract

After electrical breakdown, full recovery of electrical performance in Ru metal nanocrystal-based high-κ/SiO_2 non-volatile memory gate stack is realized with a simple electrical method. The recovery mechanism is explained by the release and transport of oxygen ions from metal/oxide interfaces and the passivation of oxygen vacancies selectively in the breakdown percolation path of gate dielectric layers under gate recovery biasing. This work opens the prospect of on-chip electrical programming to realize extra margin in device lifetime of metal nanocrystal-based non-volatile memory device.

Introduction & Experimental Details

Metal-oxide-semiconductor (MOS) structure employing metal nanocrystal (MNC) has been proposed as a next generation charge-trapping non-volatile memory (NVM) [1]. In this work, we study the recovery (RC) of Ru MNC-based gate stack of 6nm Al_2O_3 (high-κ block oxide)/4nm SiO_2 (tunnel oxide) layers on n-Si substrate after breakdown (BD) of the dielectric layers. The top gate electrodes are Au dots with 300nm thickness and 160μm diameter. Fig. 1 shows the TEM cross-section of the stack. The randomly distributed Ru MNCs locate above the SiO_2 and are embedded in the Al_2O_3 layer. The planar view TEM of Fig. 2 shows the individual MNCs with mean diameter of about 3nm and number density of $3x10^{12}$ cm^{-2} [2]. BD of the gate stack was realized by a K-cycle successive constant voltage stressing [3] with a gate voltage (V_g) of ±7V. As shown in Fig. 3, a compliance current limit (I_{max}) in the range of 100nA~10μA was used to arrest the device at different BD hardness [3]. The gate leakage current (I_g) at pre-BD was about 10pA. Recovery (RC) was activated by a low voltage (V_{rec}) of +4V or -4V for 20s. After each BD or RC event, the gate stack integrity was accessed by relaxation current (I_{relax}) [4] which was measured immediately after the removal of an initializing voltage of ±3V for 5s.

Recovery of Post-Breakdown MNC-based Stack

A. Positive RC voltage: RC of Al_2O_3 layer for soft BD

Fig. 4 shows the I_g and I_{relax} of the fresh, low I_{max} (200nA) soft BD and recovered device. The fresh I_g-V_g curve shows significant hysteresis (inset) indicating charging/discharging of the MNCs, i.e., the memory function. After BD, the hysteresis disappears and $|I_g|$ at $|V_g| = 2V$ increases by more than 2 orders of magnitude. MNCs have lost charging capability because of the dielectric BD of Al_2O_3 and SiO_2 layers, i.e., a conductive percolation path is formed [5] through the stack for charges to leak. After RC at $V_{rec} = +4V$, $|I_g|$ at $|V_g| = 2V$ decreased by 5 times, indicating "partial repair of the BD path".

The contribution of the SiO_2 layer to the whole stack I_{relax} is negligible because of its small magnitude and decay time compared to that of high-κ layer [6]. Thus I_{relax} reflects primarily the dielectric integrity of the Al_2O_3 layer. It can be seen from Fig. 4(b) that the fresh I_{relax} follows a typical dielectric relaxation behavior of Curie-von Schweidler law: $\boldsymbol{I = at^{-n}}$ [4]. This behavior is not seen after BD. After RC, I_{relax} becomes similar to that of the fresh device, indicating that the high-κ (Al_2O_3) layer has re-gained its insulator property. However, $|I_g|$ is still 10 times larger than that of the fresh device (Fig. 4(a)), demonstrating that the SiO_2 layer is still broken down.

B. Negative RC voltage: full RC for soft BD

Fig. 5 compares the I_g and I_{relax} of the device recovered by two RC events both with V_{rec} = -4V after two low I_{max} soft BDs (I_{max} = 200nA and 100nA, respectively). Fig. 5 shows that after a RC event (i.e., RC#2) immediately from second BD event (i.e., BD#2), both the I_g and I_{relax} are recovered to resemble the fresh-like performance.

C. Bipolar RC voltage: full RC for hard BD

Fig. 6 compares the I_g and I_{relax} trends after 3 RC events with V_{rec} = +4V and -4V for a case of 2 successive hard BDs (high I_{max} of 10μA in BD#1 and 5μA in BD#2, respectively). Fig. 6 shows that the I_g magnitude, I_g-V_g hysteresis and I_{relax} behavior are all fully recovered to fresh-like, after the third RC event (i.e., RC#3).

Physical Mechanism of Recovery in MNC-based Stack

Fig. 7 is the proposed model of observed recoveries. We previously reported that upon electrical BD in a gate dielectric layer, a percolation path consisting of oxygen vacancies (V_o) is formed (Fig. 7(b)), resulting in large I_g [7]. The amount of V_o in the percolation path increases with BD hardness [8-9]. The expelled oxygen travel in the form of ions (O^{2-}), and can be trapped in the potential wells of the metal/oxide interfaces: Au gate/oxide and Ru MNC/oxide [10]. They act as two types of O^{2-} reservoirs. Given the fact that the MNCs are nano-spheres with average diameter of about 3nm (Fig. 2) and a density of ~$3x10^{12}$ cm^{-2}, the MNC/oxide interface has larger effective surface area per unit volume than that of the gate/oxide interface and hence stores a larger amount of O^{2-}. V_o could either be neutral or positively charged (V_o^{2+}, electrons depleted). Under a negative V_{rec} (Fig. 7(c)), the neutral V_o are depleted, increasing the capture cross-section of O^{2-}, while the O^{2-} de-traps from the two O^{2-} reservoirs and travel towards the anode side (substrate). Because of the larger amount of trapped O^{2-} and smaller work function (hence shallower potential well for O^{2-} to de-trap) of the MNC material (Ru, 4.71eV) compared to the gate (Au, 5eV), more O^{2-} ions are released from the MNC/oxide interfaces than that of the gate/oxide. V_o annihilation is realized when an electron depleted V_o^{2+} captures an O^{2-} ($V_o^{2+} + O^{2-} = O_o$) [11]. Thus minor and major V_o annihilation occur in the top Al_2O_3 and bottom SiO_2 layers respectively. While under a positive V_{rec} (Fig. 7(d)), only O^{2-} in the MNC/oxide interface can move towards the anode side (gate). Whereas the O^{2-} ions at the Au gate/Al_2O_3 interface cannot penetrate into the Au gate as interstitial defects or form oxide with Au, thus they remain at the interface. V_o annihilation happens only in the top Al_2O_3 layer. The percolation path in Al_2O_3 and SiO_2 layers can then be "switched off" when enough V_o are passivated to prevent electron-hopping. The amount of V_o in the percolation path of soft BD is relatively small, so the application of only negative V_{rec} (minor and major repair in Al_2O_3 and SiO_2) could enable a full RC (the Fig. 5 case), while positive V_{rec} causes RC only in the Al_2O_3 high-κ layer (the Fig. 4 case) . For hard BD, V_{rec} of both polarities are required to fully passivate the percolation path in the two oxide layers (the Fig. 6 case).

The proposed model is further supported by a control experiment on a similar device with only a few Pd MNCs (evident by TEM and EDX measurements in Fig. 8). Coupled with the larger work function of Pd (5.12eV), this MNC/oxide interface with less MNCs was inadequate to provide significant de-trapped O^{2-} ions required to recover the BD path and hence we found that no full RC could be achieved (not shown) for this device.

Conclusion

The phenomena of recovery of Ru MNC-based Al_2O_3/SiO_2 NVM gate stack after soft and hard BDs are studied. Polarity-dependent oxygen vacancy annihilation in the BD percolation path of the constituent Al_2O_3 and SiO_2 dielectric layers by oxygen ions released from the gate/oxide and MNC/oxide interfaces is proposed as the recovery mechanism.

References: [1] Z. Liu *et al., Tran. on Elec. Devi.*, **49**, 1606 (2002). [2] P. K. Singh *et al., Elec. Devi. Lett.*, **29**, 1386 (2008). [3] V. L. Lo *et al., Elec. Devi. Lett.*, **27**, 396 (2006). [4] A. K. Jonscher, *J. Phys. D: Appl. Phys.*, **32,** 57 (1999). [5] J. Sune *et al., Thin Solid Films*, **185**, 347 (1990). [6] H. Reisinger *et al., IEDM'01,* pp267. [7] X. Li *et al., Appl. Phys. Lett,*. **93**, 072903 (2008). [8] X. Li *et al., Appl. Phys. Lett.*, **93**, 262902 (2008). [9] X. Li *et al., Appl. Phys. Lett.*, **94**, 132904, (2009). [10] B. Gao *et al., IEDM '08,* pp.4. [11] W. H. Liu *et al., IEDM'09,* pp.135.

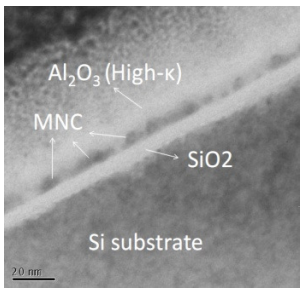

Fig. 1 TEM micrograph showing the cross-section of device gate stacks with Ru MNCs embedded at the Al_2O_3/SiO_2 interface.

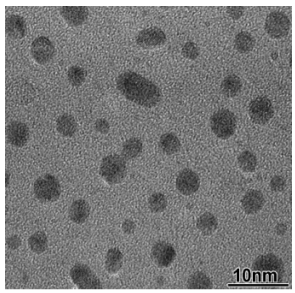

Fig. 2 Planar TEM showing the individually embedded MNCs.

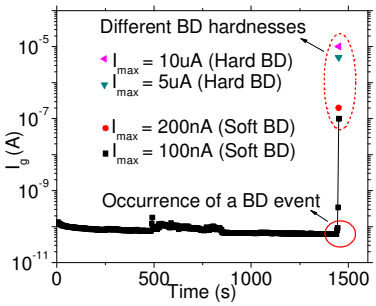

Fig. 3 The plot of gate leakage current I_g vs. time showing different hardness of BDs arrested at different compliance current I_{max}.

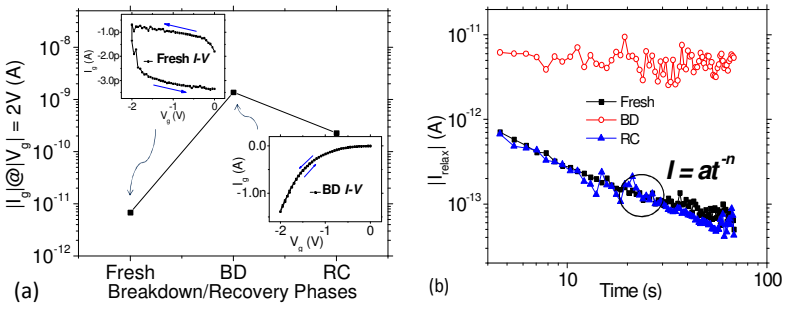

Fig. 4 **Partial** RC of **soft** BD with **positive** RC voltage: (a) $|I_g|$ at $|V_g|$=2V (the insets show hysteresis in fresh I_g-V_g, but not in the BD I_g-V_g), (b) I_{relax} of fresh device, after BD and after RC. The BD event used V_g = -7V and I_{max} = 200nA. The RC event used V_{rec} = **+4V**.

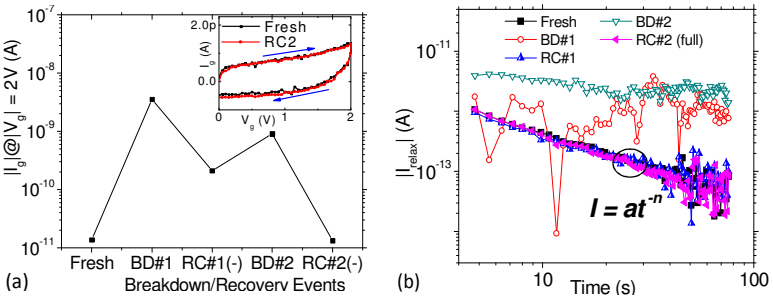

Fig. 5 **Full** RC of **soft** BD with **negative** RC voltages: (a) $|I_g|$ at $|V_g|$=2V (the inset shows that the fully recovered I_g-V_g resembles fresh device), (b) I_{relax} of fresh device, after BD and after RC; V_g = 7V, I_{max} = 200nA and 100nA, respectively in BD#1 and BD#2 events. V_{rec} = **-4V** in both RC#1 and RC#2**.**

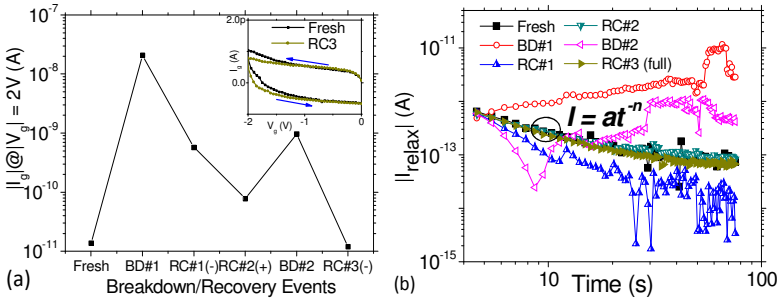

Fig. 6 **Full** RC of **hard** BD with **dual polarity** RC voltages: (a) $|I_g|$ at $|V_g|$=2V (the inset shows that the fully recovered I_g-V_g resembles fresh device). (b) I_{relax} of fresh device, after BD and after RC; the BD#1 and BD#2 used V_{gs} = -7V, I_{max} = 10μA and 5μA, respectively. RC#1 (V_{rec} = **-4V**) and RC#2 (V_{rec} = **+4V**) were performed after BD#1 and RC#3 (V_{rec} = **-4V**) was performed after BD#2.

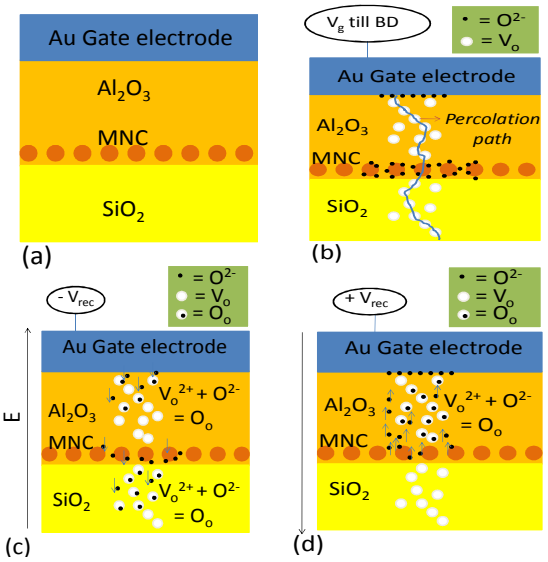

Fig. 7 Schematic models showing the Au/Al_2O_3(MNC embedded)/SiO_2/Si stack under (a) fresh condition, (b) BD condition (c) negative V_{rec}, leading to minor and major V_o annihilation in Al_2O_3 and SiO_2 layers respectively, and (d) positive V_{rec} providing V_o annihilation only in Al_2O_3 layer.

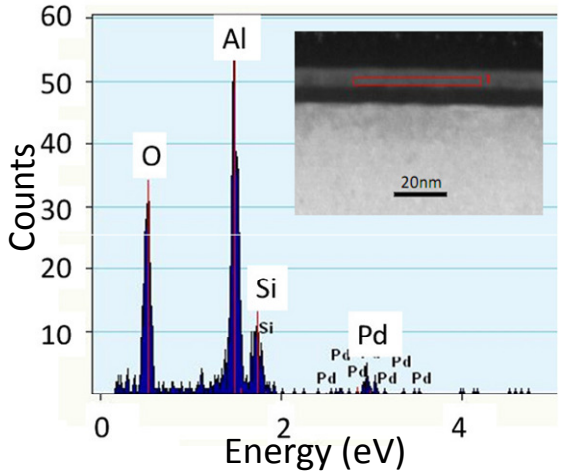

Fig. 8 EDX horizontal line scan of the Al_2O_3 layer containing Pd MNC revealing a low Pd count (inset of cross-sectional TEM shows the scan area).