POST-BREAKDOWN RECOVERABLE METAL NANOCRYSTAL-BASED AL₂O₃/SIO₂ GATE STACK FOR NON-VOLATILE MEMORY

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Abstract

After electrical breakdown, full recovery of electrical performance in Ru metal nanocrystal-based high-$\kappa$/SiO$_2$ non-volatile memory gate stack is realized with a simple electrical method. The recovery mechanism is explained by the release and transport of oxygen ions from metal/oxide interfaces and the passivation of oxygen vacancies selectively in the breakdown percolation path of gate dielectric layers under gate recovery biasing. This work opens the prospect of on-chip electrical programming to realize extra margin in device lifetime of metal nanocrystal-based non-volatile memory device.

Introduction & Experimental Details

Metal-oxide-semiconductor (MOS) structure employing metal nanocrystal (MNC) has been proposed as a next generation charge-trapping non-volatile memory (NVM) [1]. In this work, we study the recovery (RC) of Ru MNC-based gate stack of 6nm Al₂O₃ (high-$\kappa$ RuO₂ oxide)/4nm SiO₂ (tunnel oxide) layers on n-Si substrate after breakdown (BD) of the dielectric layers. The top gate electrodes are Au dots with 300nm thickness and 160µm diameter. Fig. 1 shows the TEM cross-section of the stack. The randomly distributed Ru MNCs locate above the SiO₂ and are embedded in the Al₂O₃ layer. The planar view TEM of Fig. 2 shows the individual MNCs with mean diameter of about 3nm and number density of 3x10$^{12}$/cm$^2$ [2]. BD of the gate stack was realized by a K-cycle successive constant voltage stressing [3] with a gate voltage ($V_g$) of ±7V. As shown in Fig. 3, a compliance current limit ($I_{\text{limit}}$) in the range of 100mA-10µA was used to arrest the device at different BD hardness [3]. The gate leakage current ($I_g$) at pre-BD was about 10µA. Recovery (RC) was activated by a low voltage ($V_{\text{rec}}$) of +4V or -4V for 20s. After each BD or RC event, the gate stack integrity was accessed by relaxation current ($I_{\text{relax}}$) [4] which was measured immediately after the removal of an initializing voltage of ±3V for 5s.

Recovery of Post-Breakdown MNC-based Stack

A. Positive RC voltage: RC of Al₂O₃ layer for soft BD

Fig. 4 shows the $I_g$ and $I_{\text{relax}}$ of the fresh, low $I_{\text{limit}}$ (200mA) soft BD and recovered device. The fresh $I_{\text{rec}}$-V curve shows significant hysteresis (inset) indicating charging/discharging of the MNCs, i.e., the memory function. After BD, the hysteresis disappears and $I_g$ at $|V_g|$ = 2V increases by more than 2 orders of magnitude. MNCs have lost charging capability because of the dielectric BD of Al₂O₃ and SiO₂ layers, i.e., a conductive percolation path is formed [5] through the stack for charges to leak. After RC at $V_{\text{rec}}$ = +4V, $I_{\text{relax}}$ at $|V_g|$ = 2V decreased by 5 times, indicating “partial repair of the BD path”.

The contribution of the SiO₂ layer to the whole stack $I_{\text{relax}}$ is negligible because of its small magnitude and decay time compared to that of high-$\kappa$ layer [6]. Thus $I_{\text{relax}}$, reflects primarily the dielectric integrity of the Al₂O₃ layer. It can be seen from Fig. 4(b) that the fresh $I_{\text{relax}}$ follows a typical dielectric relaxation behavior of Curie-Weiss-Schneider law: $I_{\text{relax}}$ ∝ $t^a$ [4]. This behavior is not seen after BD. After RC, $I_{\text{relax}}$ becomes similar to that of the fresh device, indicating that the high-$\kappa$ (Al₂O₃) layer has re-gained its insulator property. However, $I_{\text{relax}}$ still 10 times larger than that of the fresh device (Fig. 4(a)), demonstrating that the SiO₂ layer is still broken down.

B. Negative RC voltage: full RC for soft BD

Fig. 5 compares the $I_g$ and $I_{\text{relax}}$ of the device recovered by two RC events both with $V_{\text{rec}}$ = -4V after two low $I_{\text{limit}}$ soft BDs ($I_{\text{limit}}$ = 200mA and 100mA, respectively). Fig. 5 shows that after a RC event (i.e., RC#2) immediately from second BD event (i.e., BD#2), both the $I_g$ and $I_{\text{relax}}$ are recovered to resemble the fresh-like performance.

C. Bipolar RC voltage: full RC for hard BD

Fig. 6 compares the $I_g$ and $I_{\text{relax}}$ trends after 3 RC events with $V_{\text{rec}}$ = +4V and -4V for a case of 2 successive hard BDs (high $I_{\text{limit}}$ of 10µA in BD#1 and 5µA in BD#2, respectively). Fig. 6 shows that the $I_g$ magnitude, $I_g$- $V_g$ hysteresis and $I_{\text{relax}}$ behavior are all fully recovered to fresh-like, after the third RC event (i.e., RC#3).

Physical Mechanism of Recovery in MNC-based Stack

Fig. 7 is the proposed model of observed recoveries. We previously reported that only a few Pd MNCs (evident by TEM and EDX measurements in Fig. 8) on the anode side (gate). Whereas the O₂ ions at the Au gate/Al₂O₃ interface cannot penetrate into the gate as interstitial defects or form oxide with Au, they remain at the interface. $V_o$ annihilation happens only in the top Al₂O₃ layer. The percolation path in Al₂O₃ and SiO₂ layers can then be “switched off” when enough $V_o$ are passivated to prevent electron-hopping. The amount of $V_o$ in the percolation path of soft BD is relatively small, so the application of only negative $V_{\text{rec}}$ (minor and major repair in Al₂O₃ and SiO₂) could enable a full RC (the Fig. 5 case), while positive $V_{\text{rec}}$ causes RC only in the Al₂O₃ high-$\kappa$ layer (the Fig. 4 case).

For hard BD, $V_{\text{rec}}$ of both polarities are required to fully passivate the percolation path in the two oxide layers (the Fig. 6 case). The proposed model is further supported by a control experiment on a similar device with only a few Pd MNCs (evident by TEM and EDX measurements in Fig. 8). Coupled with the larger work function of Pd (5.12eV), this MNC/oxide interface with less MNCs was inadequate to provide significant de-trapped O₂ ions required to recover the BD path and hence we found that no full RC could be achieved (not shown) for this device.

The phenomena of recovery of Ru MNC-based Al₂O₃/SiO₂ NVM gate stack after soft and hard BDs are studied. Polarity-dependent oxygen vacancy annihilation in the BD percolation path of the constituent Al₂O₃ and SiO₂ dielectric layers by oxygen ions released from the gate/oxide and MNC/oxide interfaces is proposed as the recovery mechanism.
(a) The inset shows that the fully recovered Fig. 6 = 10 of fresh device, after BD and after RC; the BD#1 and BD#2 used performed after BD#1 and BD#2 events. respectively in BD#1 and BD#2.

Fig. 1 TEM micrograph showing the cross-section of device gate stacks with Ru MNCs embedded at the Al2O3/SiO2 interface.

Fig. 2 Planar TEM showing the individually embedded MNCs.

Fig. 3 The plot of gate leakage current I vs. time showing different hardness of BDs arrested at different compliance current Imax.


Fig. 4 Partial RC of soft BD with positive RC voltage: (a) I-V at |V|/2V (the insets show hysteresis in fresh I-V, but not in the BD I-V), (b) Imax of fresh device, after BD and after RC. The BD event used Vg = -7V and Imax = 200nA. The RC event used Vrec = +4V.

Fig. 5 Full RC of soft BD with negative RC voltages: (a) I-V at |V|/2V (the inset shows that the fully recovered I-V resembles fresh device), (b) Imax of fresh device, after BD and after RC; Vg = 7V, Imax = 200nA and 100nA, respectively in BD#1 and BD#2 events. Vrec = -4V in both RC#1 and RC#2.

Fig. 6 Full RC of hard BD with dual polarity RC voltages: (a) I-V at |V|/2V (the inset shows that the fully recovered I-V resembles fresh device), (b) Imax of fresh device, after BD and after RC; the BD#1 and BD#2 used Vg = -7V, Imax = 10µA and 5µA, respectively. RC#1 (Vrec = -4V) and RC#2 (Vrec = +4V) were performed after BD#1 and RC#3 (Vrec = -4V) was performed after BD#2.

Fig. 7 Schematic models showing the Au/Al2O3(MNC embedded)/SiO2/Si stack under (a) fresh condition, (b) BD condition (c) negative Vrec, leading to minor and major Vg annihilation in Al2O3 and SiO2 layers respectively, and (d) positive Vrec providing Vg annihilation only in Al2O3 layer.

Fig. 8 EDX horizontal line scan of the Al2O3 layer containing Pd MNC revealing a low Pd count (inset of cross-sectional TEM shows the scan area).