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Investigation of Threshold Voltage Disturbance Caused by Programmed Adjacent Cell in Virtual Source/Drain NAND Flash Memory Device

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1. Introduction

Recently, mobile applications are demanding high density NAND flash memory. The issues of the equivalent oxide thickness (EOT) scaling down of flash cells due to the data retention, however, make it difficult to reduce the short channel effect (SCE) in the deep submicron regime [1]. As one of the promising candidates, virtual source and drain (VSD) structure has been introduced and reported to overcome this problem [2][3]. Fig. 1 shows its typical schematic diagram.

However, this structure has some disturbance of threshold voltage due to fringing field induced by charge of programmed adjacent cell. The fringing field induced by charge in adjacent memory node inhibits the inversion of virtual source/drain region. So, it increases the threshold voltage of the read cell, as illustrated in Fig. 2. This is especially the drawback for the multi-level cell (MLC) operation. Because the level-to-level V_{TH} margin is narrower in the MLC than the single-level cell (SLC), small threshold voltage variation can induce a read error [4][5]. In this paper, we investigate the threshold voltage disturbance caused by programmed adjacent cell in virtual source/drain NAND flash memory device. By the device simulator, we simulate the VSD NAND flash memory device and observe the threshold voltage disturbance. And we also fabricate the VSD arch NAND flash memory device for observing and minimizing the disturbance.

2. Device Simulation

To analyze the V_{TH} disturbance of the array, simulation was performed by Silvaco ATLAS. The schematic diagram of simulated SONOS NAND array structure is shown in Fig. 3. The array structure has virtual source and drain (no n^+-doped region between the cell gates). The flash memory cells are connected in series with two select transistors. The bottom oxide / nitride / top oxide thicknesses of flash cells are 3nm / 6nm / 6nm. Fig. 4 shows the threshold voltage disturbance of the simulated memory device as a function of cell gate length. Threshold voltage disturbance increases as the cell gate length decreases. It's because the short channel effect enhances the threshold voltage disturbance. And the threshold voltage disturbance also increases, as the VSD length decreases. When the VSD length decreases, the inversion layer of VSD region is influenced much more by the fringing field of charge in programmed adjacent cell. The conventional NAND flash memory device which has n^+ doped source/drain is less disturbed by programmed adjacent cell. We can see that the VSD inversion layer is weaker when the adjacent cell is programmed. (Fig. 5)

3. Device Fabrication and Experimental Results

To verify this, the arch VSD NAND flash devices which have various VSD length (WL gap) are fabricated by silicon processing. On p-type (100) wafers, ion implantation process was performed to adjust threshold voltage. Next, the active region was defined by the e-beam lithography process and patterned through dry etch process. Just after this step, rounding process was performed to form the arch shape using chemical dry etch (CDE) as shown in Fig 6(a). ONO stack was formed by a consecutive LPCVD process. After the formation of an ONO layer, doped poly silicon for the word line was deposited. After that, the doped poly silicon layer is etched to a half of the deposited thickness. Oxide was deposited through MTO process and then an oxide spacer is formed on the sidewall. At this step, the thickness of the oxide sidewall spacer can be controlled, thus gates and WL gaps which have various lengths can be made. After forming the spacer, the etching process of the remaining poly-Si was resumed. And then, oxide was deposited to fill the WL gap through the LPCVD. Fig. 6(b) is the SEM image after formation of bit line and word line patterns. The fabricated array has 2 bit lines, 3 word lines, and 2 select lines. After the gap fill, ion implantation was performed. The oxide between WLs blocked the ion implantation, so no n^+ doped region is inside the array. Fig. 7(a) and 7(b) shows the schematic diagram and bird's eye view of the fabricated array.

Fig. 8 shows the transfer characteristics of the fabricated device. The measured device has 80 nm cell gate length and 20 nm VSD length. The I-V characteristics are confirmed before the measurement of the threshold voltage disturbance. We have measured the disturbance after adjacent cell program (V_{TH} shift : 3V) using FN tunneling. Fig. 9 shows the threshold voltage disturbance as a function of VSD length. As previously stated, the threshold voltage disturbance increases as the VSD length and the cell gate length decreases. This verifies the previous simulation results and also means that the scaling of NAND flash memory cell further increases the threshold voltage disturbance in the VSD structure.

The disturbance problem can be minimized by the electric field concentration of the arch shape structure. The electric field concentration induced by the arch shape makes the higher fringing field at virtual source and drain

region, so it can counterbalance the influence of fringing field induced by charge in adjacent memory node. Fig. 10 shows the threshold voltage disturbance as a function of BL width. As the arch fin width decreases, the V_{TH} disturbance decreases. This can be explained by the fact that the thinner arch fin is influenced much more by the field concentration effect due to the arch shape. This result demonstrates the minimization of the threshold voltage disturbance by the arch-shape.

4. Conclusion

In this paper, we investigate the threshold voltage disturbance caused by programmed adjacent cell in VSD NAND flash memory device. The device simulation and measurement data of fabricated devices show that the disturbance increases as the cell gate length and VSD length decreases. And it can be minimized by the electric field concentration induced by the arch shape structure.

Acknowledgements

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References

[1] P. Xuan, et al., IEDM Tech. Dig., pp. 609-612, 2003.
[2] H. T. Lue, et al., VLSI Tech. Dig., pp. 140-141, 2008.
[3] C. H. Lee, et al., VLSI Tech. Dig., pp. 118-119, 2008.
[4] H. Nitta, et al., IRPS Tech. Dig., pp. 307-310, 2009.
[5] T. Kim, et al., *IEEE Solid-State Electronics*, vol. 53, pp. 792-797, 2009.

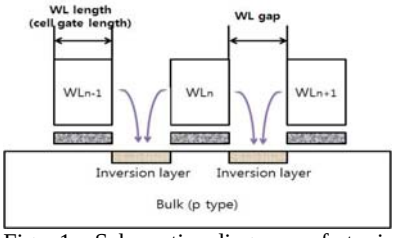


Fig. 1. Schematic diagram of typical NAND flash memory using virtual source and drain.

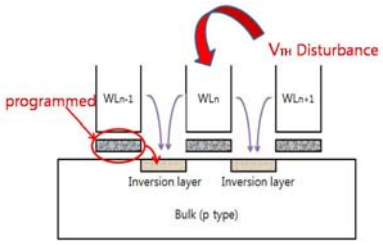


Fig. 2. Threshold voltage disturbance caused by programmed adjacent cell in VSD NAND flash memory.

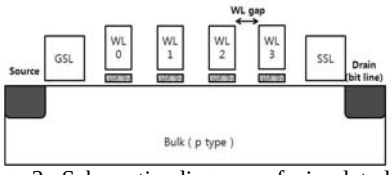


Fig. 3. Schematic diagram of simulated virtual S/D NAND flash memory.

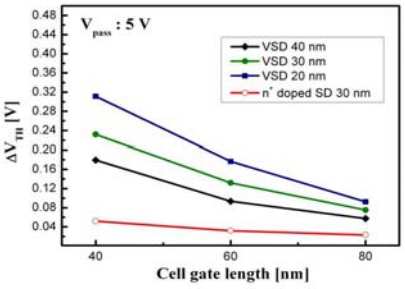


Fig. 4. Simulated threshold voltage disturbance as a function of cell gate length.

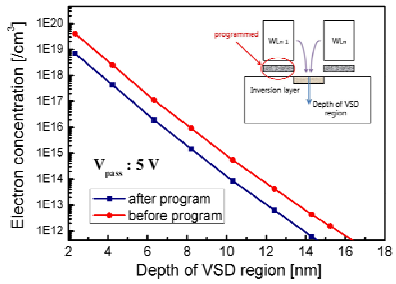
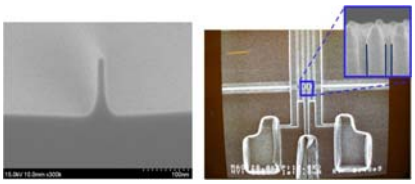
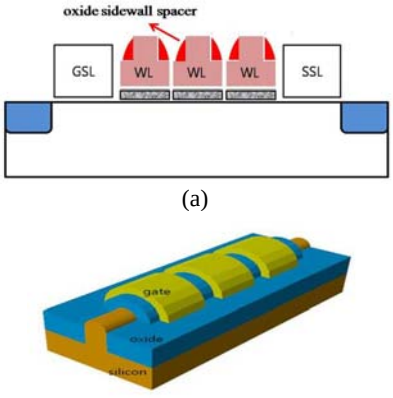


Fig. 5. Simulated electron concentration of the VSD region after adjacent cell program.



(a) (b)

Fig. 6. SEM image of (a) arch Si fin right after the CDE process and (b) the fabricated array after formation of bit line and word lines.



(a)

(b)

Fig. 7. (a) Schematic diagram and (b) bird's eye view of the fabricated array.

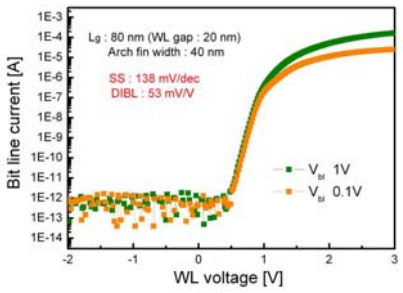


Fig. 8. Transfer characteristics of the fabricated arch VSD NAND array. (measurement data)

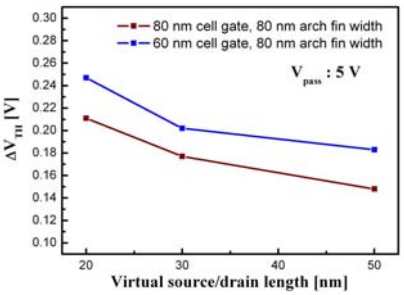


Fig. 9. Measured threshold voltage disturbance as a function of VSD length.

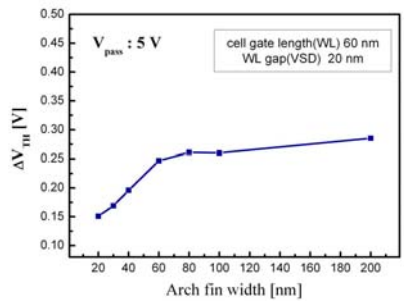


Fig. 10. Measured threshold voltage disturbance as a function of arch fin width (BL width). This shows the disturbance is minimized due to the electric field concentration effect.