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Band Energy Engineered Metal Nanodots Nonvolatile Memory to Achieve Long Retention Characteristics

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1. Introduction

Metal nanodots (MND) memories are considered as candidates for further scaling nonvolatile memories [1]. In particular, metals have various work functions so there are a lot of flexibilities for band energy design. In this work, gate band energy engineering of MND memories was investigated, systematically. It is an effective method to improve the memory properties, especially the retention characteristics. At first, the single layer MND memory was band energy engineered by choosing different work-function MND. Furthermore, the double stacked MND memory with band energy engineering was proposed. The memory characteristics were evaluated in detail.

2. Band energy engineering of single MND memory

Self-assembled nanodots deposition (SAND) method was employed to form MND embedded in silicon oxide matrix. High resolution transmission electron microscopy (HRTEM) images of cross-sectional cobalt nanodots (Co-ND) and tungsten nandots (W-ND) films were showed in Fig. 1. The MNDs with high density (Co-ND: $5x10^{12}/cm^2$, W-ND: $1x10^{13}/cm^2$) and small size (1-2nm) were confirmed Here, the work function of Co-ND is ~5.0eV and that of W-ND is ~4.5eV.

The MIS memory capacities with single MND floating gate were fabricated. The structures are as below:

1. p-Si substrate (280 μm)/SiO_2 (5 nm)/Co-ND (2 nm) /SiO_2 (1 nm)/HfO_2 (40 nm) /Al (1 μm).
2. p-Si substrate (280 μm)/SiO_2 (5 nm)/W-ND (2 nm) /SiO_2 (1 nm)/HfO_2 (40 nm)/Al (1 μm).

Figure 2 and 3 show the C-V curves of Co-ND and W-ND MIS memory capacitors, respectively. The large hysteresis memory windows were found. It indicates the charge injection into or from MNDs. In this work, the electron injection was evaluated, which response to the positive shift of flat band voltage. Figure 4 shows the retention time as function of substrate baking temperatures. Here, the retention time was defined as the time when the loss of charged electron is 20%. At room temperature (298K), the retention time of Co-ND MIS memory capacitor is larger than the case with W-NDs by 24 times because of the large work-function. For Co-ND with work function of ~5.0eV, the tunneling probability of electron will be lower than that of W-NDs with work function of ~4.5 eV by 3 orders, which calculated by WKB approximation. Based on above result, we fabricated Co-ND MOSFET memory by gate last process to investigate the memory properties. Figure 5 shows the process flow. The gate stack structure is that p-Si substrate/SiO_2 (5 nm)/Co-ND (2 nm)/SiO_2 (1nm)/HfO_2 (40 nm)/Ta (60 nm). Fig. 6 shows drain current (Id)–gate voltage (Vg) characteristics of the Co-ND MOSFET memory. The channel length is 1.5 μm and width is 10 μm. The large threshold voltage shift of 3.6V was obtained by programming at 8V. Fig. 7 shows the charge retention characteristic. The shift of threshold voltage of 2.0 V was still remained at 10 years retention. It is large enough for nonvolatile memory application.

3. Band energy engineering of double stacked MND memory

We also proposed a double stacked MND memory with band energy engineering. The schematic of cross-sectional structure was showed in Fig. 8. The top layer MND2 is Co-ND with high work-function, and bottom layer MND1 is W-ND with low work-function. As shown in Fig. 9, at program state, the electrons are mainly stored in MND2 due to the large potential well. In retention state, the difference of work-function between MND1 and MND2 supplies an additional barrier for charged electrons in MND2. It prevents the tunneling out of electrons to silicon substrate and improves the retention properties.

The W-ND/Co-ND double stacked MND MIS capacitor was fabricated. The HRTEM image of stacked MND structure was showed in Fig. 10. Also, as reference, the Co-ND/Co-ND double stacked MND MIS capacitor was fabricated. These structures are as following.

3. p-Si substrate (280 μm)/SiO_2 (5 nm)/W-ND (2 nm) /SiO_2 (3 nm)/Co-ND (2 nm) /SiO_2 (1 nm)/HfO_2 (40 nm)/Al (1 μm).
4. p-Si substrate (280 μm)/SiO_2 (5 nm)/Co-ND (2 nm)/SiO_2 (3 nm)/Co-ND (2 nm)/SiO_2 (1 nm)/HfO_2 (40 nm)/Al (1 μm).

Fig. 11 shows the flat band voltage shift as function of program gate voltages. For Co-ND/Co-ND case, flat band voltage shift finally becomes larger than that of the single Co-ND. It indicates that the electrons are injected to both top Co-ND and bottom Co-ND layers. But for W-ND/Co-ND case, flat band voltage shift is smaller than the single Co-ND. It means electrons were mainly injected to the top Co-ND layer only as our band engineering theory. Fig. 12 shows the comparison of retention characteristics between double and single MND memory capacitors. Here, the shift of flat band voltage was normalized by that value at retention time of 100s. It was found that the retention characteristic of double stacked W-ND/Co-ND sample is better than both Co-ND/Co-ND and Co-ND samples. It indicates that the work-function difference between W-ND and Co-ND improved the retention characteristic as our band energy engineering concepts.

4. Conclusion

Single layer Co-ND and W-ND were formed with high density and small size. Comparing with W-ND, the Co-ND with high work function shows long retention time. The Co-ND MOSFET memory was fabricated using gate last process, which shows good memory properties. Furthermore, the W-ND/Co-ND double stacked structure was formed, successfully. Comparing with Co-ND/Co-ND structure and Co-ND structure floating gates, the W-ND/Co-ND MIS capacitor shows excellent retention characteristics. The results indicate that the band energy engineering is one of the most effective methods to realize high performance nonvolatile memory.

Acknowledgements

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References

[1] Y. Pei *et al.*, *Appl. Phys. Lett.*, **95**, 2009, 033118.

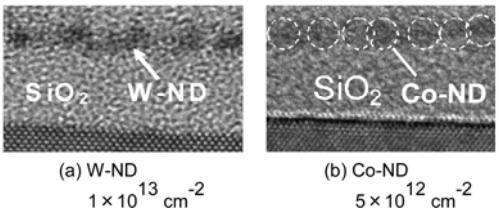

Fig. 1 Cross-sectional HRTEM image of single layer MND film.

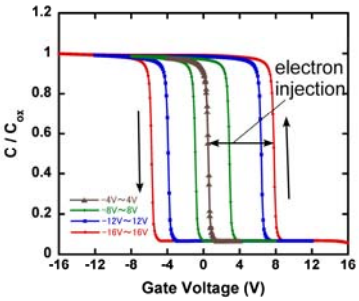

Fig. 2 C-V characteristic of Co-ND MIS memory capacitor.

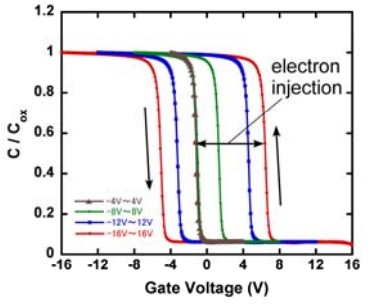

Fig. 3 C-V characteristic of W-ND MIS memory capacitor.

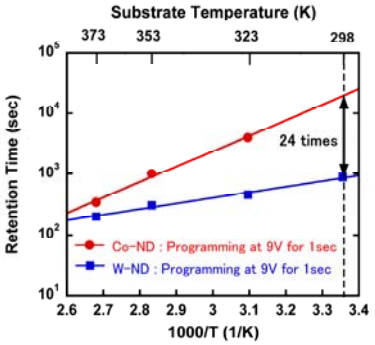

Fig. 4 Retention time as function of substrate baking temperature

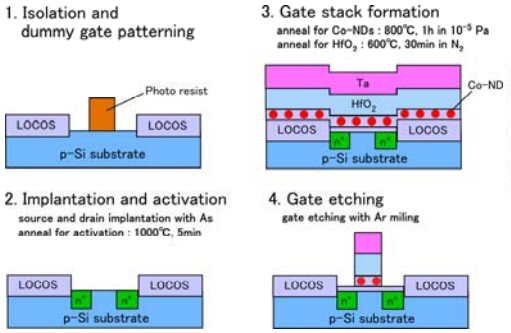

Fig. 5 Process flow of Co-ND MOSFET memory.

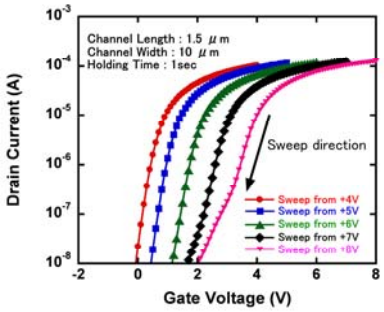

Fig. 6 Id-Vg characteristics of Co-ND MOSFET memory.

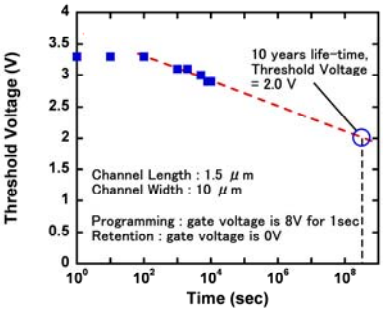

Fig. 7 Retention characteristic of Co-ND MOSFET memory.

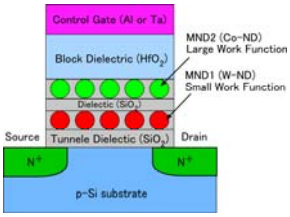

Fig. 8 Cross sectional structure of double stacked MND memory.

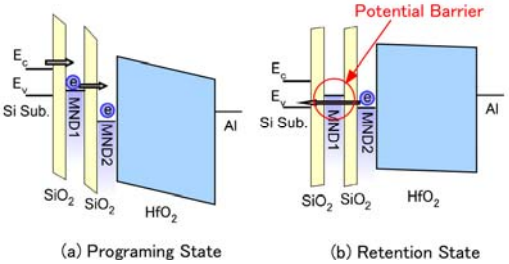

Fig. 9 Band diagram of double stacked MND memory.

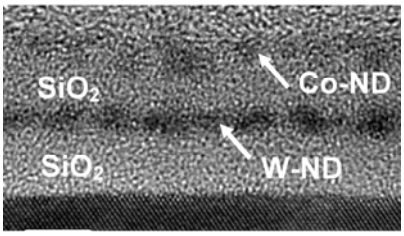

Fig. 10 Cross-sectional HRTEM image of double stacked W-ND/Co-ND film.

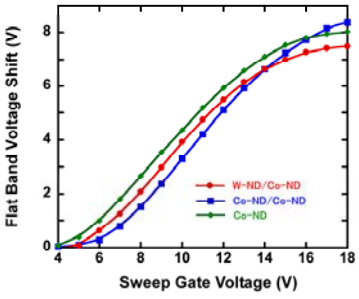

Fig. 11 Flat band voltage shift of the double stacked MIS capacitors.

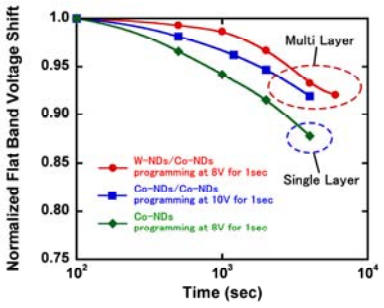

Fig. 12 Comparison of retention characteristics for double and single MND memories.