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Current Status and Future Challenge of Fe-NAND/SRAM Cell Technology

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1. Introduction

This paper overviews Ferroelectric (Fe-) NAND flash memory and Ferroelectric 6T-SRAM. The 86% power reduction in Fe-NAND increases the number of NAND chips written in parallel in SSD by 6.9 times and enhances the SSD performance up to 9.5GByte/sec. A high write/erase endurance, 100Million cycle is also realized. A ferroelectric 6T-SRAM is proposed for the 0.5V low power CPU and SoC. During the read/hold, V_{TH} of Fe-FETs automatically changes to increase SNM by 60%. During the stand-by, V_{TH} increases to decrease the leakage current by 42%. The supply voltage decreases by 0.11V, which decreases the active power by 32%.

2. Ferroelectric (Fe-) NAND Flash Memory

In the last five years, as the data through internet increases, the power consumption at the data center doubled. To solve the power crisis SSD is expected to replace HDD. For such an enterprise SSD, the Fe-NAND flash memory [1] is most suitable due to a low power consumption and a high reliability. As shown in Fig. 1(a), the Fe-NAND is composed of series-connected MFIS (Metal Ferroelectric Insulator Semiconductor) transistors (Fe-FETs). In the Fe-FET, the ferroelectric layer, $SrBi_2Ta_2O_9$ (SBT), is integrated in a gate stack of standard CMOS transistors with the metal gate, Pt and the high-K dielectric, Hf-Al-O (Figs. 1(b) and (c)). The program/erase voltage decreases from 20V of a conventional floating-gate (FG-) NAND to 6V. In the Fe-NAND, the electric polarization in the ferroelectric layer flips with a lower electric field and the threshold voltage, V_{TH} of a memory cell shifts (Fig. 1(d)). Due to a low program/erase voltage, a low power operation is achieved. Table 1 compares the conventional FG-NAND with the Fe-NAND. In the Fe-NAND, a high write/erase endurance, 100Million cycles is realized (Fig. 1(e)) because there is no stress-induced leakage current which degrades the data retention of the FG-NAND. An excellent 10year data retention is achieved by inserting a Hf-Al-O buffer layer between a ferroelectric layer and a Si substrate (Fig. 1(f)) [2]. The Fe-NAND is in principle scalable below 10nm to the crystal unit-cell size as a data is stored with an electric polarization in a ferroelectric gate insulator.

A Single-Cell Self-Boost (SCSB) program scheme is proposed [3] to achieve a 1.0V power supply operation in Fe-NAND (Fig. 2). In the proposed SCSB scheme, only the channel voltage of the cell to which the program voltage V_{PGM} is applied is self-boosted in the program-inhibit NAND string. Table 2 summarizes the program schemes. The proposed program scheme shows an excellent tolerance to the program disturb at the power supply voltage, V_{CC}=1.0V. The power consumption of the Fe-NAND at V_{CC}=1.0V decreases by 86% compared with the conventional FG-NAND at V_{CC}=1.8V without degrading the write speed. The number of NAND chips written simultaneously in Solid-State Drives (SSD) increases by 6.9 times. As a result, the 9.5GByte/sec write throughput of the Fe-NAND SSD is achieved for an enterprise application.

3. Ferroelectric (Fe-) 6T-SRAM

The proposed 6T-SRAM [4] is shown in Fig. 3. The proposed SRAM consists of 6 transistors which is identical to the conventional 6T-SRAM. The body of NMOS and PMOS are set to V_{DD} and V_{SS} to self-adjust the V_{TH} of PU1, 2 and PD1, 2 and increase SNM (Fig. 4). The forward-biased diode current in the proposed SRAM is suppressed at 0.5V V_{DD}. The V_{TH} of Fe-FETs changes by controlling the electric field between the gate and the body/channel. The Monte Carlo simulation results with 30 mV V_{TH} variation are shown in Fig. 5. In the proposed cell, SNM with the V_{TH} variation increases by 546% from 13 mV to 84 mV. SNM without the V_{TH} variation increases by 60%. Measured hold SNM and the bias condition are shown in Fig. 6. Due to the automatic V_{TH} shift, the measured SNM increases from 1.38V to 1.62V.

During the stand-by, the leakage PMOS and NMOS are automatically set to the high $|V_{TH}|$ to reduce the leakage current. Fig. 7 shows the measured leakage current. During the stand-by, as the V_{TH} of leakage transistors increases from 0.2 V to 0.3 V, the leakage current of the proposed SRAM decreases by 42%. At 0.5V V_{DD}, the optimal V_{TH} shift is 0.1V and V_{DD} of the proposed cell decreases by 0.11V. The V_{DD} scaling from 0.61V to 0.5V reduces the active power consumption, f x C x V_{DD}^2, by 32% (Fig. 8).

4. Conclusions

The Fe-NAND flash memory and ferroelectric 6T-SRAM are introduced. Fe-FET is suitable for realizing low power enterprise SSDs and low-voltage CPU and SoC applications.

Acknowledgements

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References:

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[2] S. Sakai et al., Electron Device Lett., vol. 25, pp.369-371, 2004.

[3] K. Miyaji et al., IMW, pp. 42-45, 2010.

[4] S. Tanakamaru et. al., IEDM, pp.283-286, 2009.

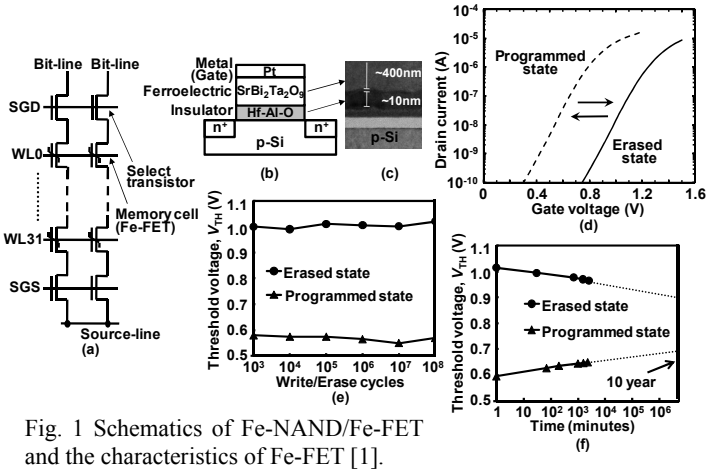

Fig. 1 Schematics of Fe-NAND/Fe-FET and the characteristics of Fe-FET [1].

	Conventional Floating-Gate NAND	Proposed Fe-NAND
Write/Erase voltage	20V	6V
Endurance	10K (MLC) 100K (SLC)	100Million
Data retention	10 years	10 years

Table 1 Comparison of conventional FG-NAND and Fe-NAND.

Program scheme	Channel voltage	V_{CC} (V)	Write energy (μJ)	NAND write speed (MB/sec)	SSD write speed (GB/sec)
FG-NAND LSB	Locally boosted	1.8	2.95 (100%)	86.2 (100%)	1.38 (100%)
Fe-NAND V_{CC} bit-line	DC biased	3.0	2.63 (89%)	95.5 (111%)	1.43 (104%)
Fe-NAND GSB	Globally boosted	3.0	2.63 (89%)	95.5 (111%)	1.43 (104%)
Fe-NAND SCSB (This work)	Locally boosted	1.0	0.42 (14%)	91.9 (106%)	9.48 (688%)

Table 2 Summary of the SCSB scheme.

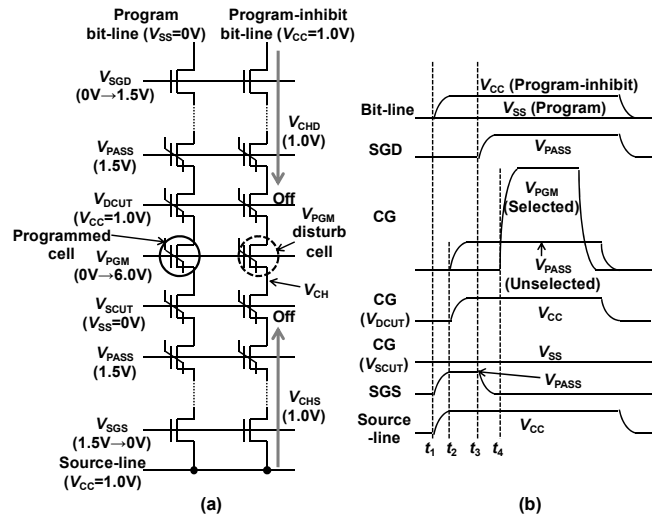

Fig. 2 (a) Proposed Single-Cell Self-Boost (SCSB) program scheme. The channel of only the selected single-cell is self-boosted. (b) Timing chart of the SCSB scheme.

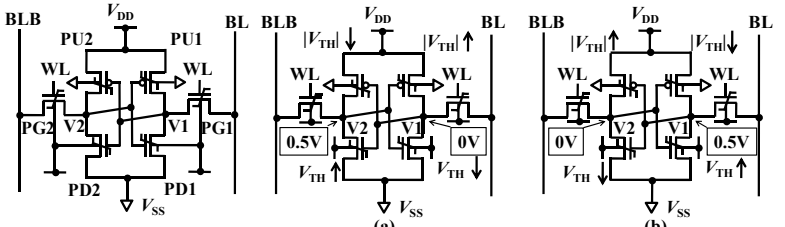

Fig. 3 Proposed Fe-SRAM.

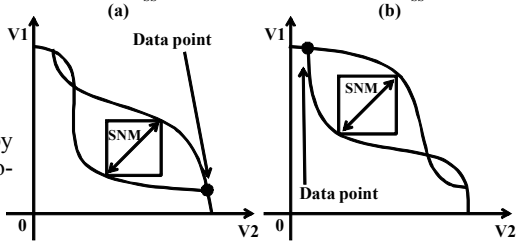

Fig. 4 SNM enhancement by V_{TH} self-adjustment in proposed SRAM.

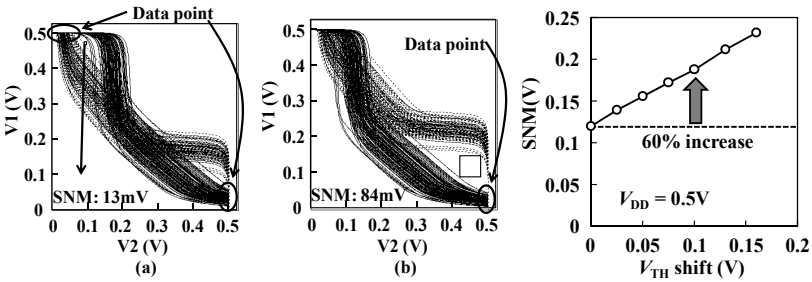

Fig. 5 Simulated SNM of (a) conventional and (b) proposed SRAM. (c) SNM enhancement as a function of V_{TH} shift.

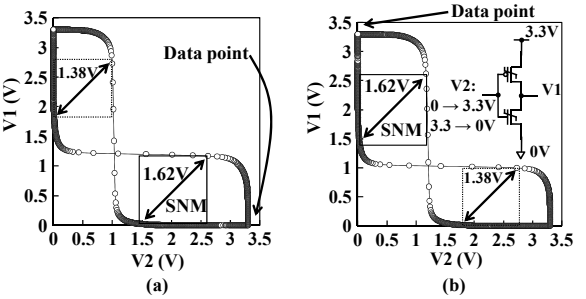

Fig. 6 Measured hold SNM in ferroelectric inverter.

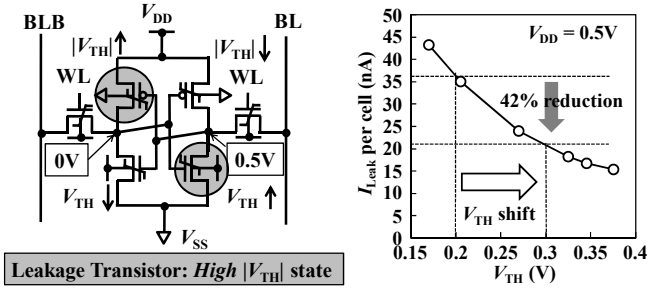

Fig. 7 Leakage current reduction in proposed SRAM.

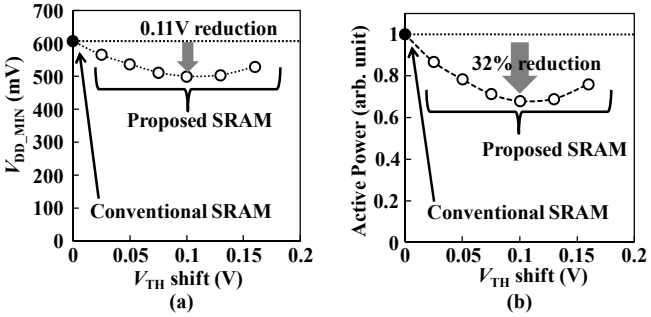

Fig. 8 V_{DDmin} reduction and active power reduction in proposed SRAM.