Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1088-1089

E-6-2(Invited)

Current Development Status and Future Challenges of FeRAM

Yoshikazu Fujimori, Hiromitsu Kimura, Yoshinobu Ichida, Jun Iida, Kinya Ashikaga, Hiroaki Ito, Takanori Ozawa, Toshiyuki Kanaya, Norihiro Kinouchi, Tatsuya Suzuki, Tomohiro Date, Daisuke Notsu, Takaaki Fuchikami, Zhong Zhiyong, Mitsuo Kojima, Masato Moriwake and Hidemi Takasu

Rohm Co., Ltd.
21 Saiin Mizosaki-cho, Ukyo-ku,
Kyoto 615-8585, Japan
Phone: +81-75-321-1457 E-mail: yoshikazu.fujimori@dsn.rohm.co.jp

1. Introduction

FeRAM (Ferroelectric random access memory) is a promising candidate for embedded non-volatile memories [1,2], because of its low-voltage and low-power operation and fast write cycle time. Now, FeRAM is used as IC card, data-logging, and some kinds of securities, but the market volume is limited because of its low capacity. We introduced non-volatile logic to widen FeRAM application [3]. By using this technology, instant boot and zero standby power are easily realized because the LSI chip retains logic states without continuous power supply [4].

In this paper, we describe process and device features of manufacturable FeRAM devices which are compatible to conventional 130nm CMOS logic process. The non-volatile logic technology and the electrical properties are also described.

2. Device feature and technology

We successfully developed an FeRAM device using a 130nm, 1.5V logic process. Figure 1 shows a cross sectional SEM view of the FeRAM. Ferroelectric capacitor module is inserted underneath first metal interconnect of conventional 130nm CMOS logic process. $Pb(Zr,Ti)O_3$ (PZT) thin film is deposited by metalorganic chemical vapor deposition (MOCVD) as the ferroelectric material. The parameters of the transistors are not changed by inserting the ferroelectric module, then we can use conventional intellectual properties (IP). Table I shows process features. The capacitor is stacked on tungsten plug and etched by one mask process to reduce FeRAM cell size. Iridium based electrodes [5] enable fatigue free high reliable capacitors. 5-level aluminum interconnects can be available in the same way of CMOS logic.

3. Non-volatile logic technology

Figure 2 shows a schematic figure of non-volatile register. A value of the register Q is stored into non-volatile ferroelectric capacitors on demand. Delay time of the register doesn't increase by adding non-volatility, because the ferroelectric capacitors are electrically separated from logic circuit by MOS transistors during logical operation. In the first non-volatile product, two pairs of ferroelectric capacitors are used as shown in Fig. 3. Two capacitors are connected in series and poled complementally, and the two pairs are used like 2T2C FeRAM in order to widen signal margin. Figure 4 shows bird's-eye view of non-volatile registers in logic circuit. Four square ferroelectric capacitors are arranged in a non-volatile register. Signal-level distribution of a 4096-non-volatile-register-chained circuit is indicated in Fig. 5. Signal margin is greater than 400mV and enough to read with high reliability. If there are some registers which have a signal margin less than quality assurance level due to the anomaly of ferroelectric capacitors, we can screen them out by electric die sort (EDS). Figure 6 shows fatigue characteristics of the ferroelectric capacitor. No fatigue loss has been confirmed at 4V up to 10^{11} cycles. Over 10^{15} cycles fatigue life time is estimated at 1.5V by voltage acceleration.

Figure 7 shows a non-volatile 4-bit counter chip. The counter logic operation is same as standard 4-bit counter and the value is stored and recalled automatically when the power turns off and on, respectively. We also prepared circuit design tools and could develop new non-volatile LSI design from a register transfer level (RTL) language circuit almost automatically.

4. Summary

We successfully developed an FeRAM technology on 130nm logic platform. The non-volatile register has wide signal margin and high endurance cycles. Reliability of data retention is guaranteed by screening out the weak capacitors in LSI testing. All logic LSI can become non-volatile one by using this technology and save electrical power and help reduce the green house gas emission.

References

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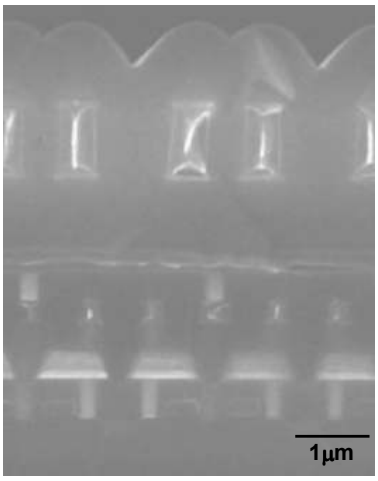


Fig. 1 Cross-sectional SEM view of FeRAM test vehicle.

Table I Process Features

Logic	130nm
Voltage	1.5V
Metallization	3 to 5-level Al
Plug	W
Ferroelectric	MOCVD PZT
Electrode Material	Ir based
Stack Etch	1Mask

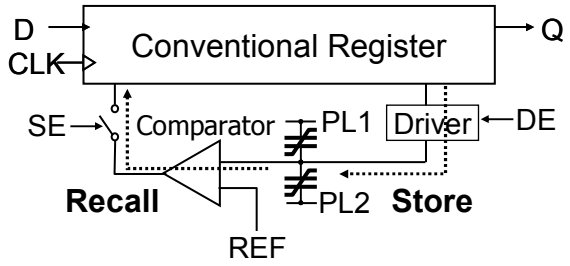
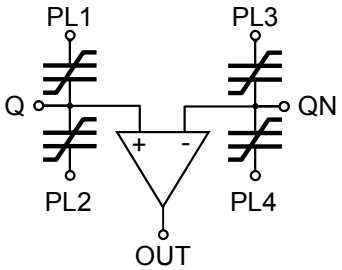


Fig. 2 Schematic figure of non-volatile register.



Operation	V_{PL1}	V_Q	V_{PL2}	V_{PL3}	V_{QN}	V_{PL4}	V_{OUT}
Write '1'	L	H	L	H	L	H	
Write '0'	H	L	H	L	H	L	
Read '1'	H	FL	L	H	FL	L	H
Read '0'	H	FL	L	H	FL	L	L

H=VDD; L=GND; FL=Float

Fig. 3 Circuit description of two pairs of ferroelectric capacitors.

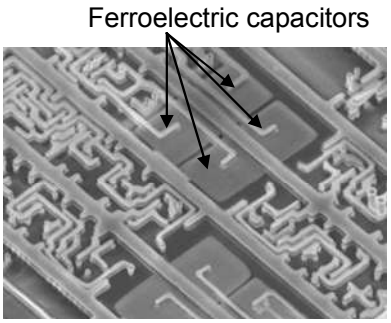


Fig. 4 Bird's-eye view of non-volatile registers in logic circuit. Square parts are ferroelectric capacitors.

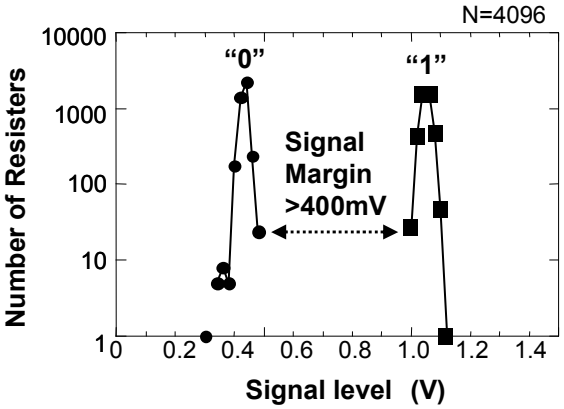


Fig. 5 Example of Signal-level distribution of 4096-non-volatile-register-chained cuircuit.

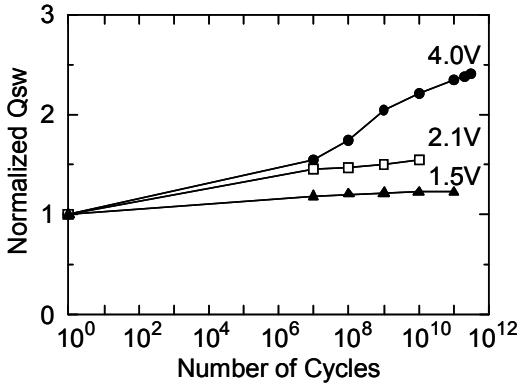


Fig. 6 Fatigue characteristics of ferroelectric capacitor.

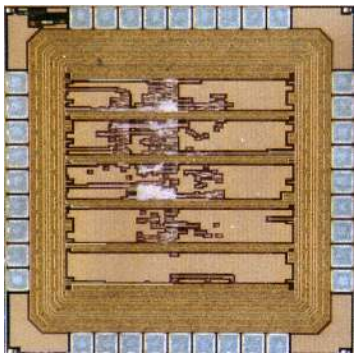


Fig. 7 Non-volatile 4-bit counter chip.