Ferroelectric-Gate Thin-Film Transistor Fabricated by Total Solution Deposition Process

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1. Introduction

Recently, various conductive metal-oxide materials have been developed, and TFTs using those materials as channels have been widely studied. Those inorganic TFTs using paraelectric materials as gate insulators are intensively studied because of their strong expectancy for flat-panel displays and system-on-panel applications [1,2]. On the other hand, when ferroelectric materials are used as gate insulators, these TFTs become nonvolatile memory transistors caused by the hysteresis property of ferroelectric materials [3-6]. These memory transistors have many advantages such as high switching speed, low-power-consumption and high integration due to the ferroelectric nature and their simple device structure. We already reported relatively good properties of ferroelectric-gate transistors (FGTs) using $(Bi, La)Ti_3O_{12}$ (BLT) or $Pb(Zr, Ti)O_3$ (PZT) film as a gate insulator and indium-tin-oxide film (ITO) as a channel [3,4].

For commercialization of these inorganic TFTs, it is indispensable to realize both high integration and ultra-low-cost fabrication. The "solution process" would be the best candidate for that purpose, because it enables good composition controllability of materials, process simplicity, low equipment costs by eliminating costly vacuum process. In order to ensure such an innovative process more effectively, it is critical to realize an all solution process in which all layers of the device are made from solution-derived materials only.

In this report, we demonstrate FGTs in which all layers are fabricated by chemical solution deposition (CSD) process using $LaNiO_3$ (LNO) film as a gate electrode, PZT film as a gate insulator and ITO film as a channel and source-drain electrodes. As far as we know, this work is the first result of an inorganic TFT fabricated by all CSD process for all layers.

2. Experimental Procedure

We fabricated a bottom gate and bottom contact source-drain structure FGT on a single crystal STO(110) substrate as shown in Fig. 1(a). Fig. 1(b) shows the plane view image of this device by a microscope. PZT which has a perovskite structure needs the same perovskite-type under layer to obtain good crystallization. For this reason, we adopted LNO film as a gate electrode. LNO is a perovskite-type conductive oxide with the lattice constant of 3.84 Å compatible with PZT (~4.1 Å). First, the $LaNiO_3$ (LNO) bottom gate (100nm) was formed by CSD. Source chemical solution of LNO was spin coated, dried at 250°C in air and then crystallized at 750°C in O_2. After that, the LNO gate was patterned by photolithography and wet-etching. Second, the $Pb_{1.2}Zr_{0.4}Ti_{0.6}O_3$ (PZT) gate insulator (225nm) was formed by CSD. Source chemical solution of PZT was spin coated, dried at 240°C in air and consolidated at 400°C in air. Then, the gate contact hole was formed by photolithography and wet-etching. After that, the PZT film was crystallized at 650°C in air. Third, the ITO source-drain electrodes (120nm) were formed by CSD. Source chemical solution of ITO (5% Sn-doped) was spin coated, consolidated at 300°C in air and patterned by photolithography and wet-etching. After PZT surface was treated by Ar dry-etching, the ITO source-drain electrodes were crystallized at 625°C in air. Fourth, the ITO channel (20nm) was formed by CSD. Source chemical solution of ITO (5% Sn-doped) was spin coated, consolidated at 300°C in air and patterned by photolithography and wet-etching. Then, ITO film was crystallized at 450°C in air. The channel length (L_{SD}), channel width (W) and gate electrode width (L_G) of the fabricated device were 5-30µm, 60µm and 50µm, respectively. Structural characterization of films was carried out by X-ray diffraction (XRD) analysis. The resistivity and carrier density of the LNO and ITO films were measured by the van der pauw method using Hall-effect measurement system (Accent HL5500). The transfer characteristics (I_D-V_G) and output characteristics (I_D-V_D) were measured by semiconductor parametric analyzer (Agilent 4155C).

3. Results and Discussion

Fig.2 shows the change of resistivity of LNO films (100nm) on STO(110) substrates. As the figure shows, quite low resistivity less than $5\times10^{-4}\Omega$cm, which is much lower than the reported one [7], was obtained in the film annealed at more than 600°C. From the process stability point of view, the annealing temperature of a gate electrode

should be higher than that of a gate insulator. Therefore, we annealed LNO and PZT films at 750°C and 650°C, respectively. XRD spectra taken from the PZT/LNO/STO(110) perovskite stack structure is shown in Fig.3. It is found that both LNO and PZT films had a (110) preferred oriented growth that was induced from the single crystal STO(110) substrate beneath. Fig.4 shows the resistivity and carrier density of the ITO film (20nm). As the annealing temperature is getting higher, the resistivity of the ITO film decreases monotonically, while its carrier density increased linearly. We adopted the annealing temperature of 600°C for the ITO source-drain electrodes and that of 450°C for the ITO channel. Because good conductivity is required for electrodes while a channel is required to have adequate carrier density for its complete depletion. Fig.5 shows the I_D-V_G and I_D-V_D characteristics of the fabricated device. The transistor showed a typical n-channel transfer curve with counterclockwise hysteresis loop at low operation voltage less than ±10Vdue to the ferroelectric nature of PZT gate insulator. We obtained on/off current ratio of ~10^5, memory window of ~2V and S-factor of 423mV/decade. Moreover a typical n-channel output characteristics and good drain current saturation were demonstrated as shown in Fig. 5(b). It is noticeable, however, that the on current is relatively lower than expected from ITO carrier density and PZT polarization charge. This may attribute to the deficient conductivity of the ITO source-drain electrodes, and this issue will be solved by using other high conductive materials.

4. Summary

We have fabricated a ferroelectric gate transistor (FGT) only by using solution process: every layer including a gate electrode, a gate insulator, source-drain electrodes and a channel were made from chemical solution deposition (CSD). It showed good typical n-channel memory transistor operation. Now "all solution process" instead of conventional "vacuum process" became quite possible in fabrication of inorganic TFTs. This would be a giant step toward "all printing inorganic electronics" that could bring us ultra-low-cost and minimal energy fabrication of sophisticated inorganic TFTs and memories.

References

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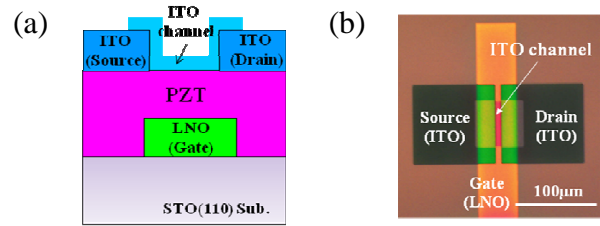
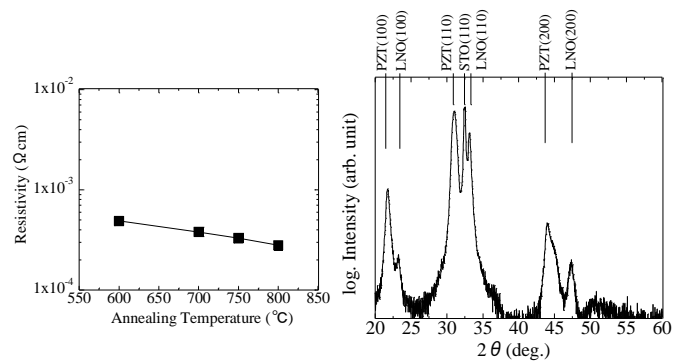Fig. 1. (a) Device structure of FGT, and (b) Plane view image of FGT by microscope.

Fig. 2. Resistivity of LNO films as function of annealing temperature.
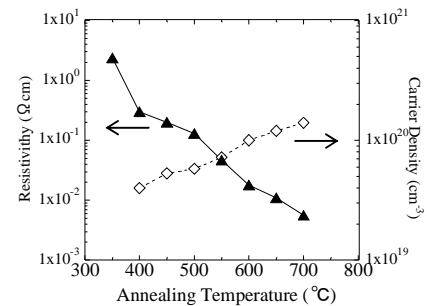

Fig. 3. XRD spectra from PZT/LNO/STO structure.

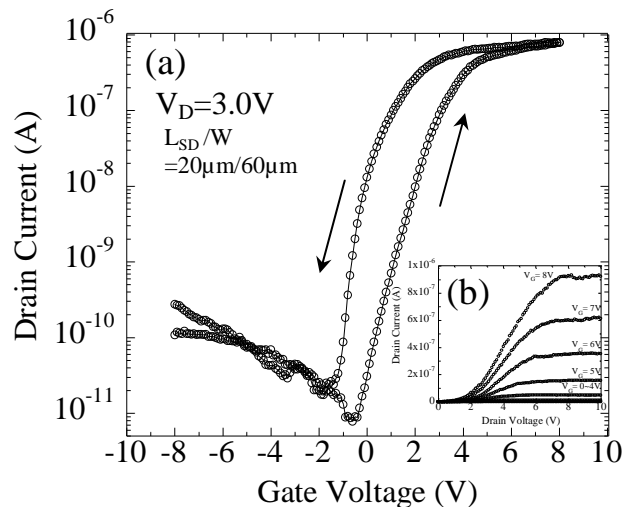Fig. 4. Resistivity and carrier density of ITO films as function of annealing temperature.

Fig. 5. (a) I_D-V_G characteristics, and (b) I_D-V_D characteristics of FGT with 10nm thickness of ITO channel.