E-7-1(Invited)

Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1094-1095

Current Status and Future Challenge of Embedded High-speed MRAM

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1. Introduction

Embedding non-volatile RAM onto SoCs has attracted growing interest since further CMOS scaling will greatly increase power consumption. Magnetic random access memory (MRAM) is the most promising candidate due to its unique features such as non-volatility, high-speed operation, and unlimited read-write endurance. This paper describes our activities and future challenges with embedded MRAM technology.

2. 2T1MTJ cell structure

Among several MRAM cell structures, the 2T1MTJ cell [1] is desirable for high-speed applications because it requires no accurate current control (Table I). We have demonstrated 250-MHz [2] and 32-Mb [3] macros with 2T1MTJ cells, where writing was performed with a magnetic field [4]. For cost performance that is comparable or superior to existing memories such as eSRAM and eDRAM, reducing write-current to less than 0.2 mA is indispensable (Fig. 1). In this viewpoint, spin-transfer torque (STT) writing is promising. In particular, the domain wall (DW) motion cell is suitable since it fits well with the 2T1MTJ structure [5].

3. DW-motion MRAM

We found that, for DW-motion MRAMs, a perpendicular magnetic anisotropy (PMA) material is preferable to an in-plane magnetic anisotropy (IMA) material because it can achieve more efficient DW motion [6]. Figure 2 shows analytical and numerical calculation results of DW motion in IMA and PMA materials. The critical current density and critical field in PMA materials are one order of magnitude smaller and larger, respectively, than the IMA materials. Furthermore, despite an increase in critical field, the current density for PMA is constant [7]. These facts suggest that, with PMA, we can achieve small cell area with sufficient stability even for fine technology generations.

We confirmed excellent writing properties of DW-motion cells with PMA materials. Figures 3, 4, and 5 show the value of write-current, switching time, and thermal stability, respectively. In these experiments, Co/Ni laminated film was used as a PMA free-layer material. In Fig. 3, the write-current reaches less than 0.2 mA at a width of less than 100 nm [8]. Also, in Fig. 4, a switching time of less than 3 ns is obtained when ℓ = 200 nm, corresponding to more than 200-MHz operation when ℓ < 100 nm. In Fig. 5, the write-current is independent of thermal stability, in agreement with the theoretical analysis.

A typical DW-motion MRAM device structure is depicted in Fig. 6 [9]. The free layer consists of three regions: two fixed regions and one data region. For writing, we use a bidirectional current and move the DW in the data region. For reading, we use tunneling magnetoresistive (TMR) effect. With this cell structure, the cell size can be as small as $12F^2$.

We fabricated 4k-array samples (Fig. 7). An initializing technique to obtain a uniform magnetic state was developed (Fig. 8). Also, good reproducible switching was demonstrated (Fig. 9).

4. Future challenge

These technologies will provide us with zero standby power consumption SoCs. Figure 10 shows an overview of a future MRAM-embedded SoC, where 5T2MTJ [10], 9T8MTJ [11], and a magnetic flip-flop (F/F) cell [12] as well as a 2T1MTJ cell can replace all types of the memory and data F/F in SoCs.

5. Conclusions

The DW-motion MRAM with 2T1MTJ cell structure has potential to replace conventional embedded memories. We confirmed its basic properties. Our technology will enable zero standby power consumption SoCs.

Acknowledgements

We thank Prof. T. Ono of Kyoto Univ. and Prof. Y. Nakatani of Univ. of Electro-Communications for their helpful advice. A portion of this work was supported by NEDO

References

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Table 1: Comparison of characteristics for typical MRAM cells. 2T1MTJ cells are suitable for high-speed applications because they have no risk of disturbance.

Architecture	Three-Terminal	Two-Terminal	
Structure	Read BL, WL, Write BLa, Write BLb	Write BL, Read WL, Write WL, Write BLa	BL, WL, BLb
Data write scheme	•Induced magnetic field •Current-induced DWM	Induced magnetic field	Spin injection
Write Read	W/R: 2T1MTJ (W/R separation)	W: Cross-point R: 1T1MTJ	W/R: 1T1MTJ
Disturb	None	Write (Half select)	Read Write (Breakdown)
Applications	High speed	Conventional	Large capacity

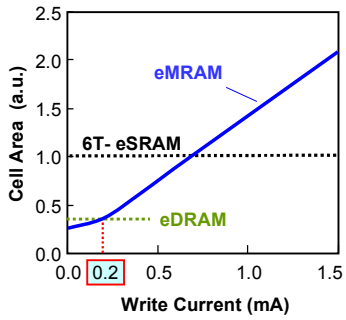

Fig. 1: Estimated cell area as a function of write-current (I_w) for 2T1MTJ cell. The cell area is mostly proportional to the write-current and it become smaller than eDRAM when I_w < 0.2 mA.

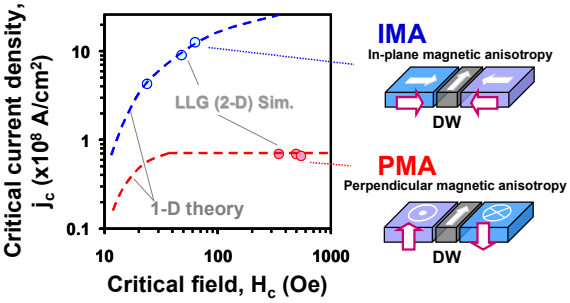

Fig. 2: Numerical and analytical calculation results for critical current density (j_c) and critical field (H_c) of DW-motion for PMA and IMA. PMA shows much smaller j_c and much larger H_c.

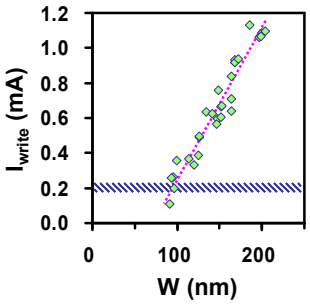

Fig. 3: Dependence of write-current (I_{write}) on width. I_{write} < 0.2 mA when w < 100 nm.

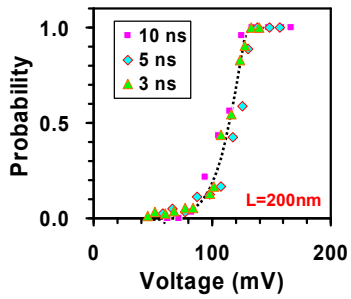

Fig. 4: Switching probability as a function of voltage for different pulse durations. 3-ns switching corresponds to >200 MHz when L< 100 nm.

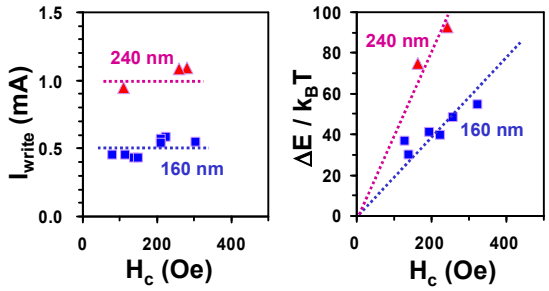

Fig. 5: Relation between I_{write} and H_c (a) and $\Delta E/k_BT$ and H_c. I_{write} was independent of H_c, whereas $\Delta E/k_BT$ was mostly proportional to H_c.

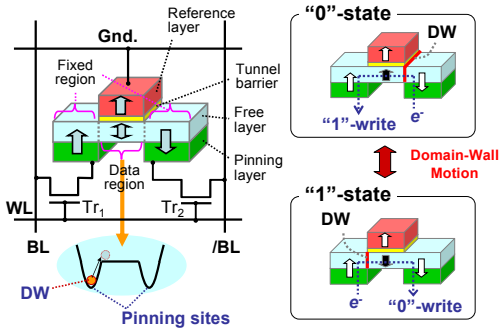

Fig. 6: Typical structure of DW-motion MRAM with PMA materials.

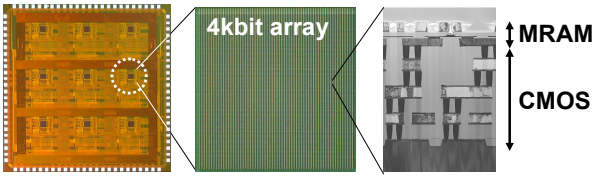

Fig. 7: Photograph and TEM image of 4k-array samples.

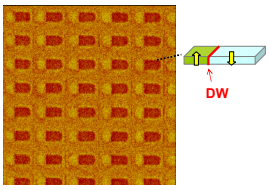

Fig. 8: MFM image of device array. Uniform state was achieved.

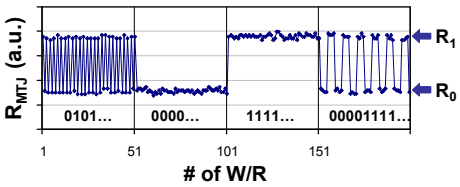

Fig. 9: Repeat test results of the device. Good reproducible switching and over-write properties were achieved

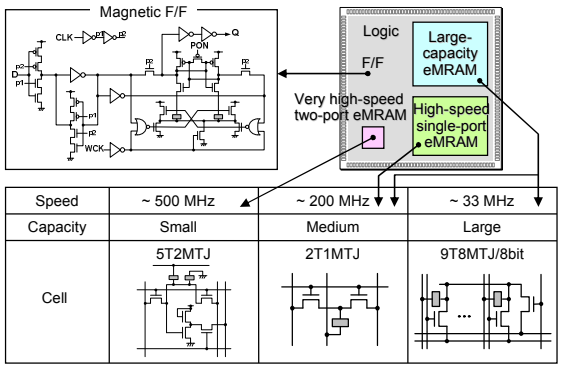

Fig. 10: Overview of an MRAM embedded SoC. All semiconductor memories and flip-flops can be replaced by MRAM cells with various cell structures.