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# A Survey of Cross Point Phase Change Memory Technologies

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## Abstract

This survey reviews the current advances in phase change memory and the integrated selector. Among all the configurations, stackable thin-film cross point memory [1-3] deliver the densest array, therefore the most compact die size. Combining its attributes in cost, performance and reliability, cross point phase change technologies stimulate potential opportunities in computing memory hierarchy.

## Introduction

In state of the art computing environments, the memory subsystem performance increases as it moves closer to processors. The relationship between cost and performance is imperative to the computing memory hierarchy, where bit capacity of each subsequent level of memory hierarchy increases by roughly one order of magnitude [4] (Table 1.)

Table 1: Cost and Performance in computing memory hierarchy

| Memory Subsystem | Normalized Parameters | | |
|---|---|---|---|
| | Cost | Throughput | Latency |
| On-chip SRAM | > 10 | > 10 | < 0.01 |
| Component DRAM | 1 | 1 | 1 |
| SSD NAND | 0.1 | 0.1 | 1,000 |
| Form factor HDD | <0.01 | < 0.01 | > 100,000 |

The performance gap between DRAM and HDD is bridged by NAND flash based SSD.

DRAM latency will be sustained and throughput will improve with Moore's Law. Predictably, NAND will continue its cost per bit strength and maintain or improve performance relative to other memories in the hierarchy. Therefore, any disruptive memory innovation to challenge the incumbents must possess performance strength within a narrow cost window between NAND and DRAM. Among all the NVM innovations, PCM technology demonstrates its maturity, scalability and robustness in integration over the others. This survey reviews cross point PCM technology basics and benchmarks against DRAM and NAND.

## Cross point Phase Change Memory Technologies

**I.** Cell size and the choice of selector: PCM arrays with different selectors have been disclosed. In a 1T1R configuration [5], the paired MOS selector limits the layout $\geq 8\lambda^2$. Using a crystalline bipolar selector [6-8], cell sizes could approach $\sim 5\lambda^2$; however, decoding CMOS circuits share the substrate with selectors, resulting in inefficient array. A self rectifying PCM [9] at $4\lambda^2$ can be implemented in a true cross point array; however, the small operating windows, the vulnerability to disturb and weak isolation between cells [10] pose a severe limitation in practice. Recent advances in two terminal thin film switches [1-3, 11, 12] enable $4\lambda^2$ cell. They are backend compatible and can be built with multiple memory decks over CMOS circuits. The cost is expected fitting into the regime of interest.

**II.** Selector I–V phenomenology: Categorized by transport mechanisms, 3 types of the thin-film devices are classified.

(1) PN junction diode [13] with rectifying switch: PN diode physics is well developed; the peak current density, pending on electronic diffusivity and leakage at reverse bias (~1pA/cell required for 10 Mb array) are below 10MA/cm$^2$.

(2) Mixed ionic-electronic conductor (MIEC) [14, 15] with bidirectional switch: MIEC is a solid electrolyte device with one electrochemically inert interface as the anode. The conduction mechanisms are based on ionic transport in electrolyte, shunted with Schottky transport. When device is biased, ions are pulled to the cathode; it leaves negatively charged vacancy as acceptor close to the anode. The acceptor concentration is modulated by bias exponentially and results in a steady state current after ~100ns of forming. It takes ~200ns to self-dissolve. The reported peak current density is > 50MA/cm$^2$ [3]. Due to bidirectional switch (see Section III and VI,) the leakage requirement of MIEC is more relaxed (3 decades higher) than that of a rectifier; ~1nA/cell at inhibiting bias point is able to support 10Mb array operations.

(3) Ovonic threshold (bidirectional) switch (OTS) [16]: The physics of OTS are fragmented [17-27]. This is partly due to the maturity of technology and the fact that device architecture has evolved over years. In addition, the conducting filaments exist only under high field in a transient of nano seconds [22, 28-30], thus equilibrium studies can be misleading. Fig.1 shows OTS quasi-static I-V characteristics. Below threshold, it exhibits a significant nonlinearity. It is Ohmic at low field and becomes exponential as field increases up to a threshold voltage. Device snaps back in Negative differential resistance (NDR) regime during switching. The ON-state exhibits high dynamic conductance with an offset. Current carrying capability matches PCM RESET requirement. Similar to MIEC, the maximum leakage allowance is ~1nA/cell at inhibiting bias point

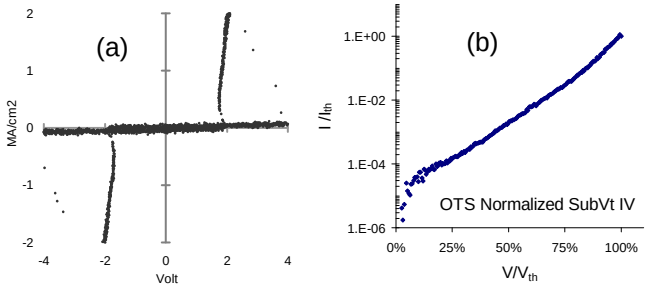


Fig. 1 (a) Quasistatic IV curves of an OTS (b) DC subthreshold IV

**III.** Array Operation: The operating principles are based on selectors' I-V nonlinearity. A rectifying selector turns on one bit with forward bias and isolates others with reverse bias (Fig. 2a). With a bidirectional selector, subject to the potential drop at each cross points, the selected bit is triggered and the unselected bits are blocked (Fig. 2b).

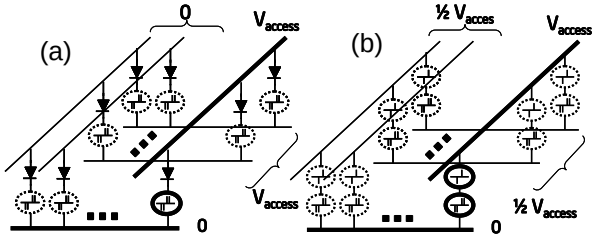


Fig. 2 cross point bias scheme for (a) rectifier based PCM & (b) PCMS

**IV.** READ: To interrogate PCM state, both PN diode and MIEC are turned ON to sense the current level. With NDR in OTS, threshold demarcation is used for read. MLC feasibility is intuitively easier with a non-NDR selector while demarcation read with a NDR is faster.

**V.** WRITE: Sub-lithographic features have been deployed to reduce RESET current. However, manufacturing latitude of those innovations becomes increasing restricted as technology scales. Also, the RESET current is converging with various device structures anecdotally [31]. The role of interfacial layers will become prominent [32]. Due to PCM's crystallization and nucleation characteristics, SET cycle time ranges from sub 100ns to 1μs. The SET current is typically less than ½ of RESET current. In an integrated cell, selector becomes the liability to cycling degradation as program current density increases. Among them, OTS shares the matched physical and electrical properties of PCM and is deemed scaling coherently. PCM's high speed vitrification capability must not be hindered by the thin-film selector in series. The WRITE voltage is comparable among all reported thin film selectors.

**VI.** Parastics: The parasitic R and C consume operating energy therefore bandwidth. The displacement current is mainly dissipated on the intra layer capacitance when accessing the bit by swinging bit-line and word-line voltages. Rectifier based arrays swing full voltage and bidirectional selector based arrays swing less. When a MIEC or an OTS based array is accessed, subject to forward blocking bias, the deselected cells in the selected column and row will consume leakage but no consumption with the rest (majority) of the bits due to equal bias on the unselected columns and rows. In contrast, in a rectifier based PCM array, most of the deselected cells are reverse biased consuming leakage power. Parasitic leakage control is imperative in technology scaling, which impacts the sizes of array partition thus cost.

**VII.** Reliability: PCM cycling endurance is > $10^9$ cycles. When integrated with selectors, due to stress tolerance subject to the thermal, chemical, mechanical and electrical properties, cycling life time of ≥ $10^6$ cycles are reported. Retention characteristics are supported by the fundamental physics of phase transformation and glass relaxation. With proper array biasing scheme design and operating voltage allocation, low operating disturbance can be achieved [29].

## Cross Point PCM in computing memory hierarchy

PCMS' [1] attributes are used to represent the class of cross point PCM technologies. Table 2 compares the attributes of PCMS projected to 34nm node against those of NAND [33] and DDR3 DRAM [34]. PCMS shares the similar cost of NAND. The access bandwidth is equal to or better than NAND's and the access latency is approaching to DRAM's. PCMS reliability is expected >100x better than NAND.

Table 2: PCMS vs. NAND and DRAM.

| Memory | | NAND MLC | PCMS SLC | DRAM |
|---|---|---|---|---|
| Normalized Cost | | 0.1 | 0.1 | 1 |
| Normalized Energy Bandwidth | READ | 1 | 1 | 1 |
| | RESET | 0.05 | 0.5 | |
| | SET* | >10 | 0.1 | |
| Normalized Access Latency | READ | 1K | 1 | 1 |
| | RESET | 20K | 3~5 | |
| | SET* | 60K | 10 | |
| Endurance (cycles) | | 10K | >1M | >1E15 |
| Disturb (cycles) | | 10K | >1E12 | N/A |

PCMS projection to 34nm is based on non-sublithographic architecture [31]. SET* is "Block Erase" for NAND.

## Conclusion

Two-terminal thin-film switches enable area efficient PCM layout. Among them, OTS possesses the most compatible scaling attributes with PCM. Integrated with CMOS, PCMS is one of the most promising NVM technologies in scalability. There exists potential opportunities for PCMS in computing memory hierarchy for future random access memory and solid state storage applications.

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