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A SiO_2 Nano-thermal Unipolar 0T-1R ReRAM Device with Built-in Diode Isolation

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I. Introduction

Resistance-based memories have gained great attention in recent years [1-3]. ReRAM typically uses a metal oxide to provide memory switching characteristics and either a transistor or a diode is needed for isolation. SiO_2 antifuse memories have been used for one-time programming (OTP) that also requires an isolation device [4].

In this work we report a unipolar ReRAM device using SiO_2 as the storage node and an in-situ formed diode as the isolation device. The process is very simple by punching through the gate oxide of a MOS capacitor. Small devices (20nm in one direction) are demonstrated, and the extremely simple process promises potential for very low cost high-density storage.

II. Structure, Experiments and Results

A. Device characteristics

Figure 1 shows the schematic diagram of the device. The structure resembles a conventional MOSFET, but without the source/drain junctions, with a thin thermal gate oxide of 1.2 nm between the N^+ poly gate and P^- substrate. A forming pulse is applied to the gate to rupture the gate oxide and a N^+/P junction is formed.

Figure 2 shows the evolutionary I-V characteristics of the 1st (forming) and subsequent RESET/SET operations. For a fresh device, we first increase the negative Vg pulse (100ns) until soft breakdown (SBD) at -6V, followed by hard breakdown (HBD) at -9V. A N+/P junction is formed after the hard breakdown. Interestingly, when Vg is further decreased to -13V, the gate current decreases ("RESET"). The resistance hysteresis can be repeated by alternately applying –7V (SET) and –13V (RESET) after the initial forming step.

Figure 3 shows the Ig-Vg curves. After the 1st HBD (forming), forward current is increased while reverse current stays low with a large ON/OFF ratio (>8 orders) typical of a PN diode. There is no need to fabricate a separate isolation device because this diode is formed in-situ, ideal for a low cost cross-point memory array. The RESET operation greatly lowers the forward current and thus allows nearly 3-orders of magnitude sensing margin. For comparison, a PN diode without gate oxide is fabricated. Figure 3 shows that the SET state read current approaches the PN diode, and the extracted ideality factor (n) is also close to each other (~1.3 to 1.4).

Figure 4 shows that the new device can be switched for nearly one hundred unipolar cycles. Figures 5-6 show that the retention and read disturb are excellent.

Figure 7 shows the transient gate currents of 1st HBD, RESET and SET states measured by pulse IV technique. Similar to most unipolar RRAM devices, RESET current is much higher than SET current.

B. Switching mechanism

The mechanism of the memory switching is clarified in this section. We first study PN diodes (without oxide) with various dimensions. Figure 8 shows that all PN diodes are permanently damaged after high voltage stressing without showing any switching behavior.

Figure 9 shows the TEM micrographs after HBD, RESET and SET operations. Poly Si from the N^+ gate breaks through the thin tunnel oxide after the HBD operation. This phenomenon has been reported as the "dielectric breakdown induced epitaxy" (DBIE) [5]. The programming current of the RESET operation causes severe local heating resulting in segregation of a thick SiO_2 layer and a poly silicon layer below. SET operation causes Si filaments in the oxide, as shown in Figs. 9(c) and (d).

The switching mechanism of device is explained in Fig. 10. The SBD operation creates percolation paths between the poly gate and the substrate. The percolation path triggers the hard breakdown and the subsequent current causes DBIE.

After the HBD, further increase in bias (RESET) results in Joule heating near the Si filament. Eventually, local temperature approaches the melting point of Si (Tcri, 1685K). Oxygen ions coming from the surrounding layer can easily drift in the molten silicon, and form SiO_2 when the current is turned off and temperature is cooled down. That's why we observed SiO_2 and partial poly Si at substrate after the RESET operation. This oxide is probably a leaky Si-rich oxide.

SET operation requires less current with lower Joule heating than the RESET operation. Si atoms are pushed by the high-momentum electron flux, and then atoms are piled up to form Si filaments, similar to electromigration. Thus SET/RESET form Si filament and SiO_2, respectively, giving rise to memory switching behavior.

Figure 11 shows resistance and temperature dependence for SET/RESET states and PN diode. SET and PN diode show similar R-T trend supporting that the SET state is indeed a PN diode.

C. Device scalability

Figure 12 shows the TEM micrographs of fresh devices in width and length directions. We have fabricated a one-sided (width direction) **20nm** MOS structure to study the extreme scaling potential.

Figure 13 compares the operation voltages and the corresponding operation currents, respectively. When device size is scaled down, the RESET voltage and RESET current are decreased. However, the current does not scale linearly with the device area. At 20nm node, it is forecasted that the RESET current is still in the mA range. More effective thermal isolation is needed to reduce the power.

III. Summary

The extraordinary memory switching characteristics of SiO_2–based ReRAM are studied for the first time. The device shows a unipolar operation and self-formed diode isolation. We further clarify that the SET operation is caused by thermally induced Si filament formation, while RESET operation is a thermal process caused by Joule heating, resulting in SiO_2 formation.

References

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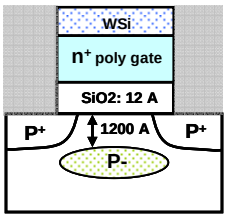


Fig. 1 Schematic of 0T1R ReRAM device. N^+ gate doping is around $8x10^{20}/cm^3$, and P^- channel doping is around $7x10^{17}/cm^3$ at a depth of 1200A.

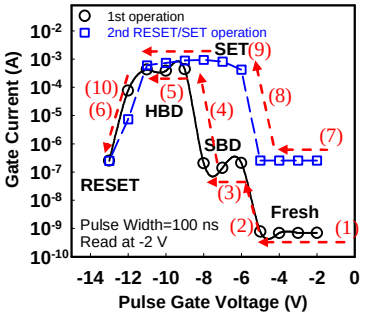


Fig. 2 Evolution of the 1st and subsequent RESET/SET operations. The arrows indicate the operation sequence. The device dimension is L/W=0.2/0.2 um.

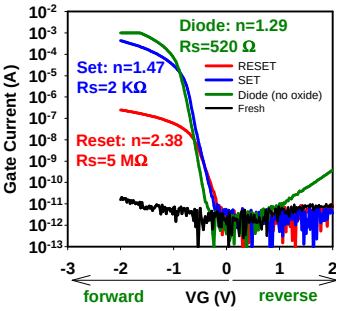


Fig. 3 Ig-Vg characteristics of cells. RESET and SET states both show diode rectifying characteristics therefore a separate isolation device in cross-point memory array is not needed.

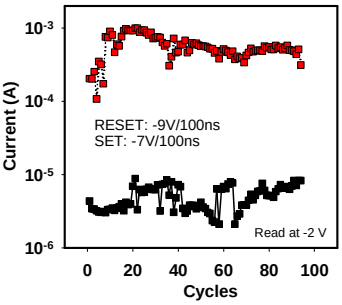


Fig. 4 Dumb mode RESET/SET cycling of a device with L/W = 130nm/20nm.

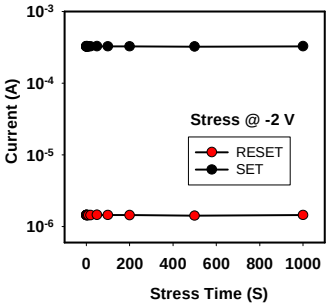


Fig. 5 Both RESET and SET states show good read disturb immunity.

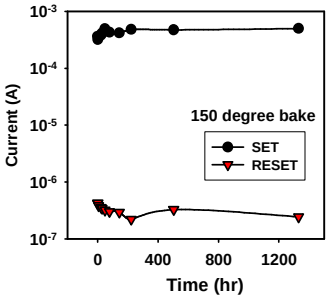


Fig. 6 High temperature retention of 0T1R ReRAM device. Both states are very stable after more than 1000-hour baking at 150 C.

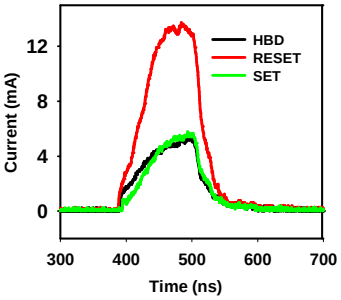


Fig. 7 Transient current of HBD, RESET and SET states. A programming width of 100 ns is used. The device dimension is L/W=0.2/0.2 um.

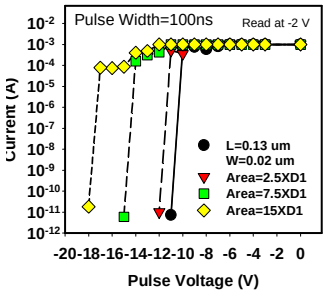


Fig. 8 Ig-Vg curves of PN diodes with various dimensions. All diodes are permanently damaged (stuck open) after subjecting to high voltage stress and did not show any switching behavior.

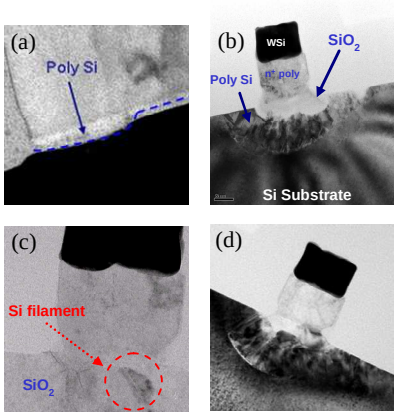


Fig. 9 TEM micrographs of 0T1R ReRAM device after (a) HBD, (b) RESET, (c) SET and (d) 100 cycles at SET, operations.

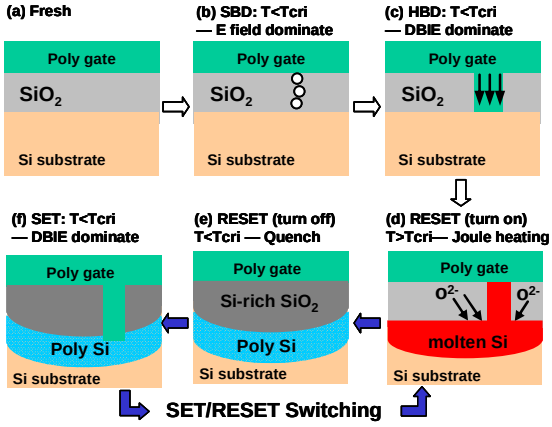
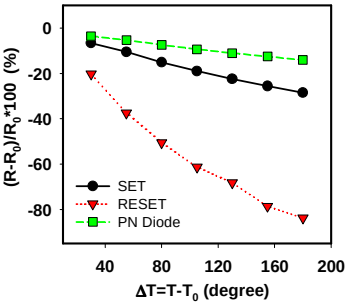


Fig. 10 Illustration of SBD-HBD-RESET-SET steps of 0T1R RRAM programming. SET operation is caused by thermally induced Si filament formation, while RESET operation is a thermal process induced by Joule heating, resulting in SiO2 formation.



T_0 (degree):room temperature, 25 degree
R_0 (Ω): Resistace at room temperature

Fig. 11 Resistance and temperature dependence for SET/RESET states and PN diode device.

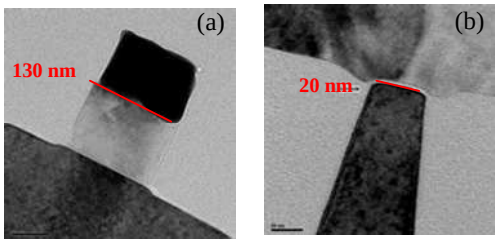


Fig. 12 TEM micrographs of fresh device in (a) length and (b) width directions. Width direction of MOS structure is 20 nm.

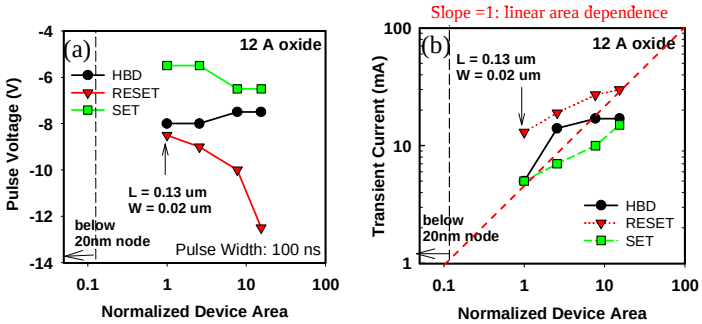


Fig. 13 Operation voltage and corresponding transient current as a function of device dimension are respectively shown in (a) and (b). When the device is scaled down, the RESET voltage and current are decreased.