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Overview and Future Challenges of Hafnium Oxide ReRAM

Y. S. Chen[1,2], H. Y. Lee[1,2], P. S. Chen[3], P. Y. Gu[1], Y. Y. Hsu[1], W. H. Liu[1], C. H. Tsai[1], S. M. Wang[1], S. S. Sheu[1], P. C. Chiang[1], W. P. Lin[1], W. S. Chen[1], F. T. Chen[1], C. H. Lien[2], and M.-J. Tsai[1]
[1]Electronics and Optoelectronics Research Laboratory, Industrial Technology Research Institute, [2]Institute of Electronics Engineering, National Tsing Hua University, [3]Department of Chemical and Materials Engineering, MingShin University of Science & Technology, Taiwan R.O.C., Phone: 886-3-5912958, Fax: 886-3-5917690, E-mail: yusheng@itri.org.tw

1. Introduction

Recently, transition-metal-oxide-based resistive random access memory (ReRAM) has emerged as a promising potential candidate for the next generation nonvolatile memory (NVM) due to its simple device structure and CMOS compatibility [1]. Among the oxide materials, HfO_2 film is used in advanced CMOS as gate insulator and is further considered to be the insulator for the ReRAM. With an appropriate reactive-metal electrode, such as AlCu, Ta, or Ti, the HfO_x ReRAM shows stable bipolar resistance switching (BRS). The HfO_x device using a thin Ti layer demonstrated excellent memory performances [2,3]. The Ti/HfO_x devices exhibit capabilities of low power and high speed operation without suffering any instability of operation parameters or unsatisfactory switching endurance [1,4]. In addition, the device is capable of multilevel operation [2] and exhibits good scalability [3]. The performance of a 1 Kb array with 1T1R configuration shows 100% device yield, very good switching performance by adequate verification schemes, and reliable endurance to approach commercialization of ReRAM technology. In this work, the characteristics of the HfO_x ReRAMs are reviewed and the challenges for this memory are also addressed.

2. Characteristics of HfO_x ReRAM

Ti/HfO_x stacked layers show robust BRS. The Ti capping layer reacted with oxygen ions of the HfO_x film and left behind with high concentration of oxygen vacancies. For the as-prepared device with thick HfO_x film (> 5 nm), a forming process is necessary to initiate resistance switching. As shown in Fig. 1, the forming voltage is linearly dependent on the thickness of HfO_x film beyond 5 nm. The device with a 3-nm-thick HfO_x film can exhibits stable BRS without a forming step. The typical BRS of this device with 1T1R configuration operated with the SET current of 200 μA is shown in Fig. 2. Both of the operation voltages (V_{SET} and V_{RESET}) are less than 1.5 V. The sensing margin is larger than 100. The resistance of the high resistance state (R_{HIGH}) and low resistance state (R_{LOW}) for the devices are higher than 1 MΩ and about 1 kΩ respectively, as shown in Fig. 3. The SET and RESET switching speeds are faster than 10 ns as shown in Fig. 4. Thus, this device is appropriate for low power and high speed operation application. The scalability of this device with the pillar structure is also be explored, as shown in Fig. 5. The BRS of the 50 nm device still exhibit large ON/OFF ratio. The V_{SET} and V_{RESET} are less than 1.5 V and insensitive to the cell size.

Figure 6 shows a typical endurance performance for this device. The cycling number can exceed more than 100 M times under repetitive SET and RESET. The sensing margin during cycling can maintain higher than 100. Figure 7 shows both R_{HIGH} and R_{LOW} of the memory device are strongly immune to the thermal disturbance and can expect to 10 years lifetime from retention tests at 150 and 220 °C. The HfO_x devices suffer a low time-to-disturb voltage of 0.4 V. By inserting an ultra-thin AlO_x between HfO_x and bottom electrode, the time-to-disturb voltage raised up to 0.5 V without any performance degradation (Fig. 8). This result is believed to be due to the reduction of applied voltage across the HfO_x layer by the AlO_x layer. Table I compares some ReRAM devices with different dielectrics. The Ti/HfO_x memory with its low operation voltage, low RESET current and high speed switching is one of the most promising candidates.

The endurances of all HfO_x devices in the 1 Kb array can exceed more than 1M times by a pulse width of 40 ns under fixed operation voltage and current as presented in Fig. 9. Compared to 1st cycling, the Weibull distributions of R_{HIGH} and R_{LOW} become more and more fluctuant with the increase of cycling number. Soft errors are found in some devices of the 1 Kb array during the SET or RESET processes. Novel verification methods [3] were proposed to effectively narrow down the fluctuation of R_{HIGH} and R_{LOW} and kept the devices with good operation window. The ON/OFF ratio of about 10 in the 1 Kb array after the verifications is depicted in Fig. 10.

3. Future challenges

There are several challenges to the HfO_x devices in the future. First, the resistance fluctuation due to the stochastic nature of resistance switching during repetitively erase/program within a high density memory array is an important concern for product reliability. The modification of device structure or composition is a direct approach to be used, which can reduce complexity and time of verification schemes for the device. The Al-doped HfO_x device is suggested to solve this problem [8]. Second, the detailed resistance switching mechanism for HfO_x device is still not cleared and needs to be explored. Although the mechanism of the ReRAM device has been studied extensively [9], still a clear switching mechanism is in great needs for designing a better and more reliable device. Finally, the bi-directional diode (bi-diode) needs to be developed for the cross-point structure in 3D stackable high-density array. Some characteristics of the bi-diode, including a large ON/OFF ratio and the current-clamp function, need to be enhanced to match the operation of the ReRAM device. In addition, a novel bipolar ReRAM device with asymmetric I-V curves for different bias polarity also shows a potential for the cross-point array application [10]. However, the resistance switching characteristics of this category of ReRAM device need to be substantially improved.

4. Conclusions

A highly reliable Ti/HfO_x ReRAM is demonstrated and integrated successfully through 1T-1R configuration with 0.18 μm CMOS technology. This memory device can switch as fast as 10 ns with large ON/OFF memory window (> 100) and low operation voltage (< 1.5 V). It also exhibits good scalability down to 50 nm and excellent reliabilities, including nonvolatility of 10 years at 220 °C and 100 M switching cycles. A 1 Kb array with robust cycling endurance (> 1M) and ON/OFF ratio of about 10 can be achieved by a pulse width of 40 ns and effective verifications. The challenges need to be overcome to realize this memory as the next generation NVM.

Acknowledgements
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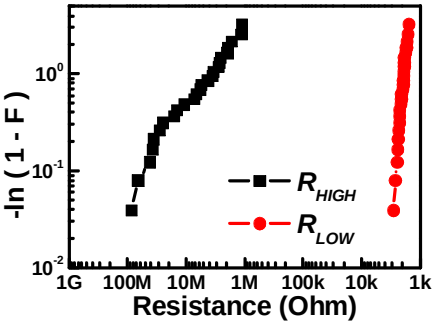

Fig. 3 Tight distribution of R_{HIGH} and R_{LOW} of TiN/Ti/HfO$_x$/TiN device in 1T1R configuration.

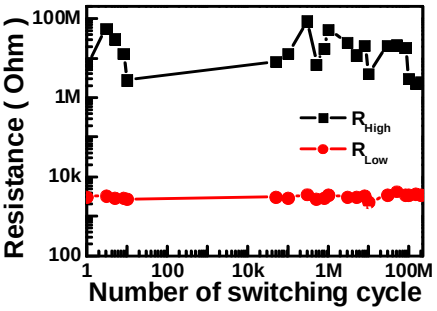

Fig. 6 Switching endurance of 100M cycles by a pulse of 40 ns.

Table I Comparison of memory characteristics for various devices with bipolar resistance switching.

Dielectric	WO_x [5]	TaO_x [6]	TiO_2 [7]	HfO_x
Top layer	–	–	Ta_2O_5	Ti
ON/OFF ratio	>10	~10	>1000	>100
V_{SET} V_{RESET}	+2.0 V -1.5 V	+2.0 V -1.5 V	+4.0 V -1.5 V	+1.5 V -1.5 V
Min. I_{RESET}	~100 uA	170 uA	200 uA	25 uA
Speed	~2 ns	10 ns	–	5 ns
Endurance	>10^8	>10^9	~10^6	>10^8
Retention	2000 hr 250 °C	10 yr 85 °C	10 yr 150 °C	10 yr 220 °C

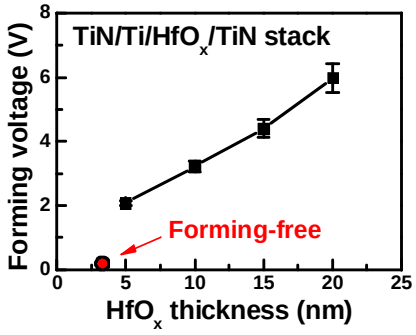

Fig. 1 HfO$_x$ thickness dependence of the forming voltage on TiN/Ti/HfO$_x$/TiN device.

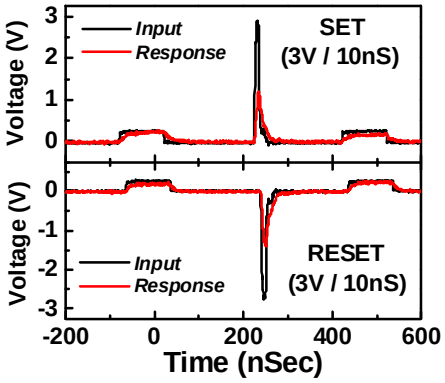

Fig. 4 Test of operation speed with 10-ns pulse width of TiN/Ti/HfO$_x$/TiN device.

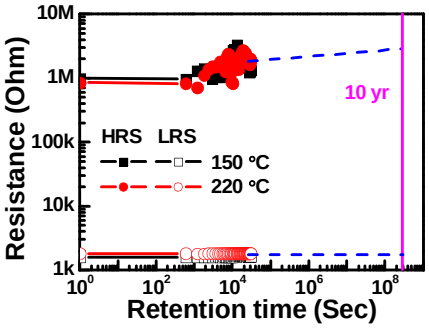

Fig. 7 Retention properties of R_{LOW} and R_{HIGH} at 150 °C and 220 °C. The result predicts 10 years lifetime of stored bit.

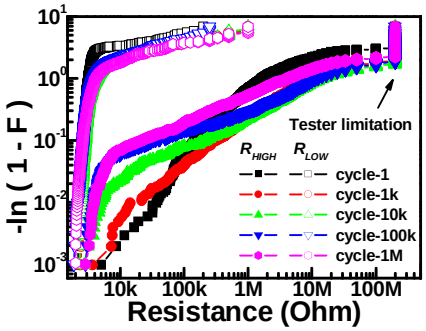

Fig. 9 R_{HIGH} and R_{LOW} distributions of all devices in the 1 Kb array by Weibull plots with cycling numbers. The endurance exceeds 1M times by 40-ns pulse.

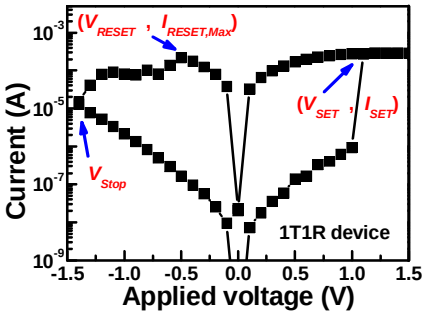

Fig. 2 Bipolar resistance switching characteristic of the TiN/Ti/HfO$_x$/TiN device in 1T1R configuration.

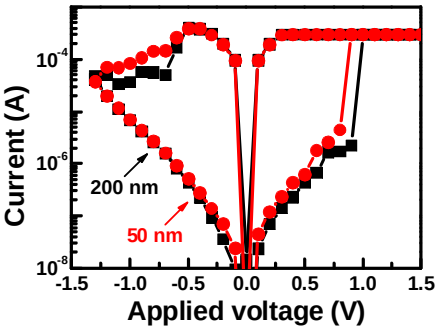

Fig. 5 Typical I-V of bipolar resistance switching of the 200 and 50 nm pillar device.

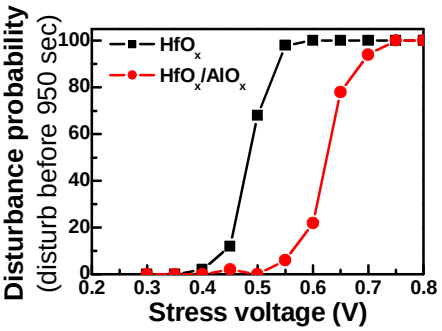

Fig. 8 Dependence of disturbance probability on stress voltage. The stress voltage is improved to 0.5 V in HfO$_x$/AlO$_x$ devices.

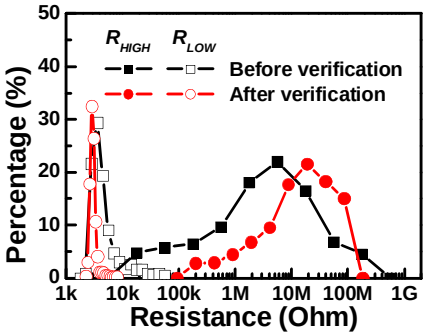

Fig. 10 Statistical distributions of R_{LOW} and R_{HIGH} of the 1 Kb array before and after effective verifications. The ON/OFF ratio is higher than 10.