Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1110-1111

High OFF/ON-resistive NiO ReRAM using Post-Plasma-Oxidation (PPO) process

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Abstract

NiO resistive change cells with a high OFF/ON resistance ratio of 10^5 are realized, in which a stoichiometry of NiO is successfully controlled by using low temperature (350ºC) post-plasma-oxidation (PPO). PPO improves a surface roughness of a PVD-NiO film, which results in reduction of a cell-to-cell variation in forming voltages, and also compensates for a loss of oxygen during BEOL process. The developed NiO ReRAM integrated in Cu-BEOL is applicable for realizing a low power switch as well as a memory.

Introduction

Nonvolatile resistive change device has attracted attention due to its simple device structure, low switching power, and small footprint [1]. Unipolar resistive change of NiO thin film is of particular interest for memory and switch applications [2]. The nonvolatile switch integrated on CMOS can enhance the device performance and power without scaling of the ULSIs [3]. NiO potentially has a high OFF/ON resistance ratio for the switch application. However, an appropriate stoichiometry of NiO for achieving the high OFF/ON resistance ratio has not been investigated yet. In this work, we have developed a high OFF/ON resistive NiO ReRAM using a low temperature post-plasma-oxidation (PPO), and have integrated the NiO ReRAM in Cu-BEOL. We also discuss effects of PPO on the resistive switching characteristics of NiO in terms of the stoichiometry of NiO.

Experimental

A. Post-Plasma-Oxidation (PPO) process

NiO thin films were deposited by PVD at 300ºC on TaN/Ru bottom electrodes under two different O_2 partial pressure conditions (HO and LO). The deposited NiO films were oxidized by N_2O/He RF-plasma at 350ºC for 60 or 300 sec (Fig. 1). Effects of PPO on the NiO films were investigated by XPS and XRR characterizations.

B. NiO ReRAM integrated in Cu-BEOL on CMOS

Under three different process conditions, NiO ReRAM was integrated into Cu interconnects on a standard CMOS (Fig. 2 and 3). A bottom electrode of TaN/Ru (5nm/5nm) was first deposited on the Cu interconnects through contact holes with the diameter of 0.2 μmϕ. Then the PVD-NiO thin film was deposited under HO or LO conditions, followed by PPO. A Ru/Ta laminated top electrode was deposited on the stack, followed by dry-etching. Next, upper-layer Cu interconnects were connected both to the stack and to the interconnects underneath through dual-damascene vias. Finally, Al pads were fabricated to probe the devices. Resistive switch characteristics were evaluated using on-chip series transistors to tune set and reset currents during the switching operations.

Results and Discussion

Compositional analysis by XPS reveals that the as-deposited PVD-NiO film has a shoulder-peak located at 853.0 eV, indicating that the NiO film partially contains metallic bindings. PPO successfully eliminates the metallic peak since the NiO film is fully oxidized by PPO (Fig. 4). The resistive switch characteristics evaluated in blanket films show that PPO decreases a forming voltage (V_F) and its distributions (Fig. 5). The XRR analysis, supposing the two-layered model after PPO, shows that the film thickness is increased and that low density surface layer is created (Fig. 6). Incorporation of oxygen atoms into the NiO film seems to generate Ni vacancy defects, resulting in the reduction of the V_F. The tight distribution of the V_F is attributed to the low surface roughness improved by PPO.

For integration of NiO ReRAM in Cu-BEOL, three kinds of process conditions (see the inserted table in Fig. 3) are applied to investigate the effects of PPO on the NiO switching characteristics after the integration. The NiO film with process C shows excellent resistive change characteristics with a high OFF/ON resistance ratio of 10^5 (Fig. 7). In this measurement, the set current of the transistor is controlled at 500 μA by manipulating the gate voltage (V_G). When the voltage applied to the top electrode is swept from 0 to +5 V, the resistive state changes to the ON-state at approximately +3 V. Next, to change the resistance to the OFF-state, the reset current of the transistor is controlled at 1.2mA by manipulating V_G. When the voltage reaches to +2 V, the current drops down to 10^{-8}A, meaning that the resistive state changes to the OFF-state.

To clarify the effect of the oxygen incorporation by PPO, the three different process conditions are compared, especially for ON-to-OFF (reset) characteristics (Fig. 8). The fully oxidized condition, process C, realizes a higher OFF-resistance state with higher reset voltage than those of the others. The effects of the incorporation of oxygen into NiO has two important roles of (i) reducing the V_F and its distribution by introducing defects and smooth surface, and of (ii) compensating the leakage path formed in NiO during the subsequent integration process (Fig. 9). The low temperature oxygen incorporation into the NiO film is a key to keep such a high OFF/ON resistance ratio.

Conclusion

The high OFF/ON-resistive NiO ReRAM is developed by using the PPO process. The incorporation of oxygen into the NiO film results in the high OFF/ON resistance ratio of 10^5. The PPO process is a useful technique to integrate the NiO ReRAM in Cu-BEOL for embedded switch and memory applications.

Acknowledgements

A part of this work was supported by the Ministry of Economy, Trade and Industry, through New Energy and Industrial Technology Development Organization (NEDO), under the Project of Strategic Development for Energy Conservation Technology.

References [1] Y. Sakotsubo et al., JJAP, 49, 04DD19 (2010), [2] M. Kawai, et al., APL, 96, 072106 (2010). [3] M. Tada et. al., IEEE IEDM pp.943 (2009).

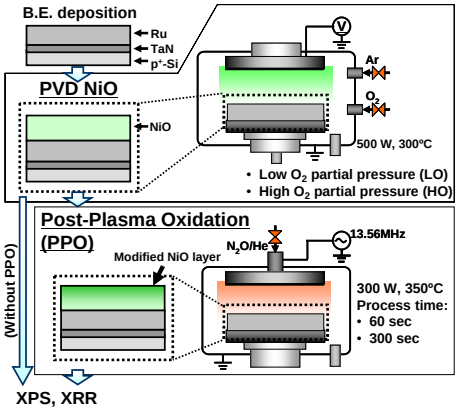


Fig.1 Schematic illustrations of PVD NiO deposition and post-plasma-oxidation (PPO) processes.

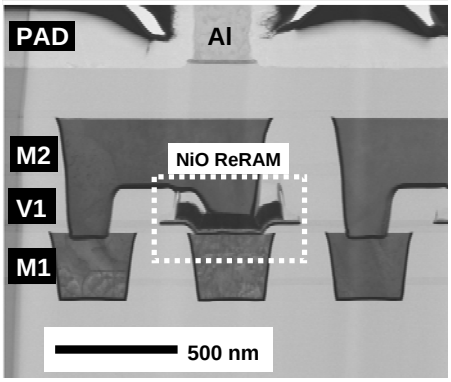
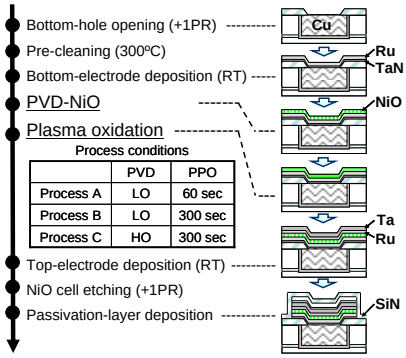


Fig.2 A cross-sectional TEM image of NiO ReRAM integrated in Cu-BEOL on CMOS.



	PVD	PPO
Process A	LO	60 sec
Process B	LO	300 sec
Process C	HO	300 sec

Fig.3 Integration process flow of the NiO ReRAM including the PPO step. The inserted table shows the process conditions for the integrated NiO ReRAM.

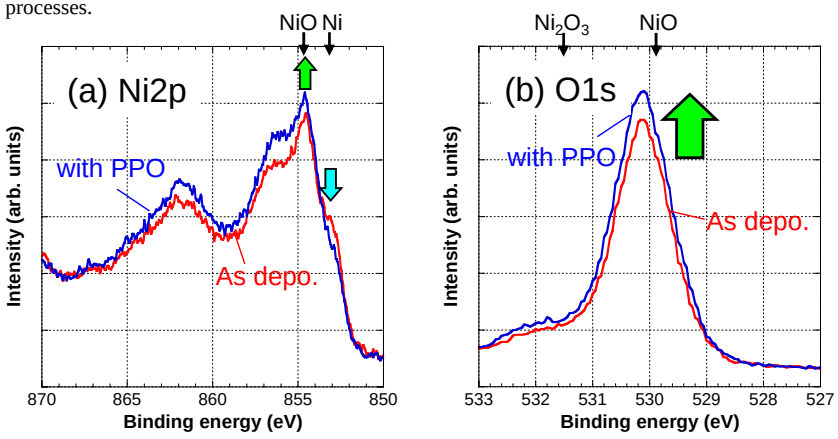


Fig.4 XPS (a) O1s and (b) Ni 2p spectra of as-deposited NiO in HO, and PPO processed NiO in process C.

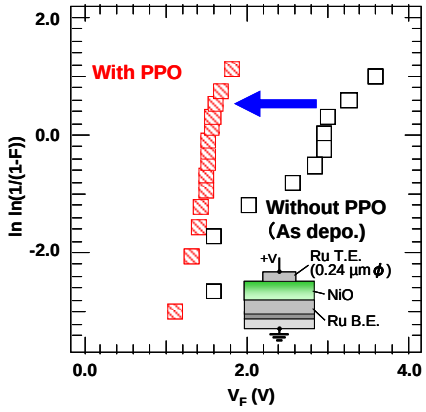


Fig.5 Distributions of the formation voltage for the NiO ReRAMs with and without PPO processes.

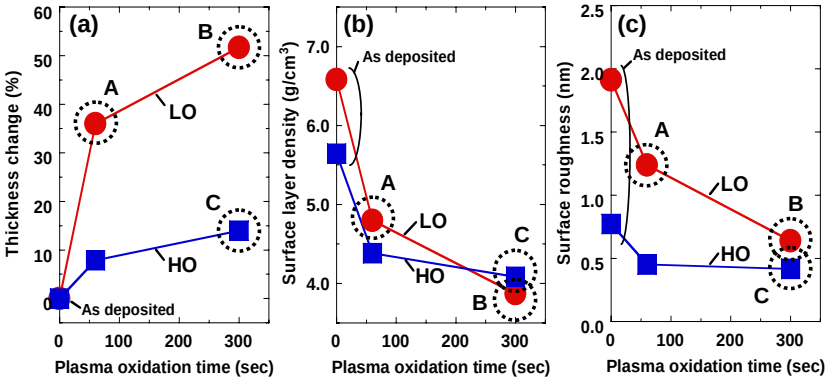


Fig.6 (a) Thickness change, (b) surface layer density, and (c) surface roughness of the PPO processed NiO films deposited under LO and HO conditions determined by XRR analysis. A, B and C process conditions shown in each graph are applied to the integrated NiO ReRAM.

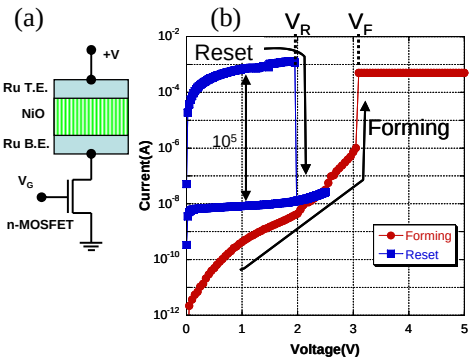


Fig.7 (a) Schematic of 1T1R configuration, (b) Typical I-V curves of the integrated NiO ReRAM processed under process C.

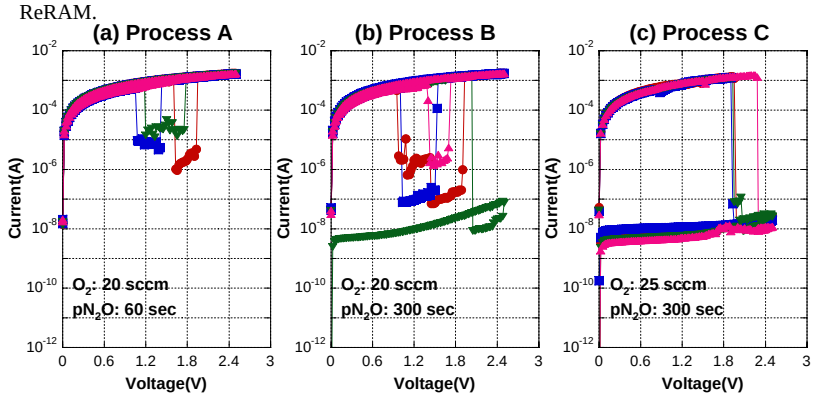


Fig.8 I-V curves of ON-to-OFF (reset) operations for the NiO ReRAMs formed under (a) process A, (b) process B, and (c) process C conditions.

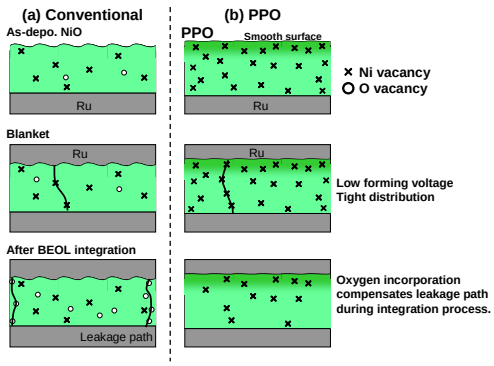


Fig.9 Schematic image of effects of the oxygen incorporation into the NiO film by the PPO process; (a) Conventional, (b) PPO.