Novel Low Power RRAM with a U-type Cell Structure for Improving Resistive Switching Characteristics

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1. Introduction
Over the recent years, there have been many studies on the “new memories” as a result of rapid progress of information technology (IT) [1]. Especially, low cost and CMOS process compatibility may enable their mass production. RRAM (Resistive Random Access Memory) is very promising in many respects, but some shortcomings such as unknown switching mechanism and high switching current, still remain [2]. In addition, it is very difficult to accomplish high density RRAM with conventional metal-insulator-metal (MIM) structure due to reset/set distribution and current compliance related large access device and high initial forming power [2].

In this paper, we propose a novel metal-insulator-metal (MIM) cell structure which makes it possible to accomplish low power RRAM for the first time. We show that controlling the size and deposition orientation of resistive material where resistive switching occurs at resistive cell material/TE interface are expected to reduce the reset current and forming voltage, which in turn efficiently controls the conducting filament (CF) results in feasibility of low power RRAM. Numerical simulation is also performed using random circuit breaker model (RCB) to confirm the proposed structure.

2. Motivation
Fig. 1 shows I-V (a) and R-V (b) curves based on our fabricated unipolar type RRAM structure [3]. Due to its structural advantages [2], we adopted unipolar RRAM with filamentary conduction path model [1] to implement high density memory. However, as shown in Fig. 2, irregular reset (a) and set (b) switching behaviors are detected intermittently with planar metal-insulator-metal (MIM) structure due to undesired conducting filament (CF) interactions [3]. We have reported that controlling the localized CF is very important to understand the unipolar resistive switching mechanism [3]. We have to consider the relationship between initial cell resistances and reset current reduction in order to implement low switching current without abnormal resistance fluctuations.

Fig. 3 demonstrates the relationships between initial resistance and reset, set and forming voltages (a), and reset, set and forming resistance (b) [3]. A unique phenomenon is that, when initial resistance is changed by novel MIM integration, forming voltage level and set voltage level become similar or forming process disappeared. By this we verified the feasibility of cell implementation without forming process. We propose a novel U-type cell structure which can easily control the CF without forming process which in turn affect initial switching results in low power RRAM.

3. Fabrication process and Results
Fig. 4 shows the schematic cross-sectional view of U-type RRAM structure, and Fig. 5 shows the schematic drawings of possible scenario of reset current reduction at planar (a) and U-type (b) RRAM structure. The number of CF associated with reset current is reduced as the contact area ‘a’ is reduced. The effect of contact area of our structure as a function of initial resistance (a) and reset current (b) is simulated. As the contact area ‘a’ shown in Fig. 5 is decreased, the initial resistance is increased. Reset current is also decreased as a function of the contact area of cell/TE interfaces. A critical contact area exists as shown in Fig. 6, thus finding optimal dimension of ‘a’ is regarded as an important factor to reduce the reset current. Fabrication process of our proposed MIM structure is depicted in Fig. 7. Once Al lower metal line, Ir bottom electrode (BE) and mold oxide such as Tetraethyl orthosilicate (TEOS) are formed, mold oxide patterning is performed step by step. After that, TiO$_2$ as resistive material and ILD material are deposited on the mold to fill the contact hole. After CMP process as shown in Fig. 7(f), Ir TE deposition and etch process are carried out to define etch cell. Finally, top electrode contact (TEC) and upper Al metal line is formed. An MIM cell structure is built in between two metal lines that are cross-pointed for selecting a resistive cell and for writing/reading data, respectively.

To test whether this proposed structure contributes to the improvement of switching characteristics, a numerical simulation is performed using random circuit breaker model (RCB), which is a dynamic bond percolation model [4]. As shown in Fig. 8, the reset current is decreased without irregular switching fluctuation to which the conventional planar MIM structure (larger contact area) is sensitive. Optimal cell thickness for reset current reduction with our structure is also examined by RCB model as shown in Fig. 9. When cell thickness is reduced, the reset current is slightly decreased compared to that of the planar type cell. However, voltage levels such as forming, reset and set states are drastically decreased as shown in Fig. 9.

Moreover, due to its unique vertical deposition orientation where current path formed, forming-less process is possible as shown in Fig. 10. This simulation and experimental data implies that proposed structure with a vertical cell
deposition process can effectively provide CF reduction, which can be used for forming-lees or low forming power RRAM.

4. Conclusions

We propose a novel RRAM structure which makes it possible to reduce the reset current by controlling the number of the electrical path occurring between electrode and resistive cell interface. Numerical simulation is also performed using random circuit breaker model (RCB) to investigate the optimal process condition. The results strongly support our proposed structure which contributes to reset current reduction with forming-less process.

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References


Fig. 1 I-V (a) and R-V (b) curves of our fabricated planar RRAM structures which show forming, reset, and set states.

Fig. 2 I-V curves showing irregular reset (a) and set (b) switching behaviors of our planar type cell structure.

Fig. 3 Initial resistance as a function of reset/set/forming voltages (a) and reset/set resistances (b).

Fig. 4 Schematic cross-section view of our edge contact top electrode (TE) RRAM structure.

Fig. 5 Possible scenario of reset current reduction in planar structure (a) and the U-type structure (b).

Fig. 6 Effect of contact area ‘a’ of U-type structure RRAM as a function of initial resistance (a) and reset current (b).

Fig. 7 Fabrication process sequence of our proposed RRAM.

Fig. 8 I-V curves of forming (a), reset and set (b) characteristics by random circuit breaker (RCB) simulation model.

Fig. 9 I-V curves of forming (a), reset and set (b) characteristics with cell thickness difference.

Fig. 10 First transition curves of conventional deposition orientation with forming (a) and our fabricated U-type structure having vertical deposition orientation with forming-less process.