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Ge nanowires for nanoscale nonvolatile memory applications

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1. Introduction

One-dimensional semiconductor nanostructures such as nanotubes and nanowires are being actively investigated for applications in electronic, photonic and sensor devices [1]. Group-IV semiconductor nanowire devices are potentially attractive because of their compatibility with existing Si complementary metal-oxide-semiconductor (MOS) integrated circuit technology. The use of floating gate memory composed of isolated dots reduces charge loss for a scaled device and improves memory characteristics such as endurance, and write/erase speeds with low operational voltage [2]. Ge quantum dot [3] based nano-floating gate memory using metal-oxide semiconductor (MOS) structures has recently attracted interest due to the potential application in next generation integrated nanoscale nonvolatile memories. The use of nanowires offers smaller operating voltages, better endurance characteristics and faster write/erase speeds, compared with conventional nonvolatile memories. In this study, the growth of Ge nanowires using VLS mechanism has been studied. The Ge nanowires in an IrO_x/Al_2O_3/Ge-NW/p-Si capacitor have been investigated for nonvolatile memory applications. The flash and resistive switching memories using Ge-NWs have been investigated for the first time. The nonvolatile memory devices under low voltage operation of <7V have been observed.

2. Experiment

Ge nanowires were grown by a vapor-liquid-solid (VLS) technique with Ge powder as the starting material (purity 99.999 %). The powder was placed in an alumina boat and inserted in a horizontal tube furnace. Silicon wafers with ultrathin gold coating as catalyst were used as substrates. The furnace was heated at 950 ^oC for 30 min under argon flow to grow the nanowires using VLS mechanism. The field emission scanning electron microscopy (FE-SEM) images were taken by a ZEISS field emission scanning electron microscope. The optical properties of the samples were studied by photoluminescence (PL) spectroscopy. The PL measurement was carried out by a Triax 320 monochromator (Jobin Yvon) and a photomultiplier detector with an excitation wavelength 325 nm. The MOS capacitors were fabricated using shadow mask to pattern IrO_x electrodes onto Al_2O_3 that had been grown on dispersed Ge nanowire. Memory devices consist of three stacked layers: blocking Al_2O_3 (25 nm), charge-storing Ge nanowire layer (nanowire diameter ~ 60-80 nm) and thin tunneling SiO_2 oxide (~ 5 nm). IrO_x has been used as a metal gate electrode. The high-frequency (1 MHz) C–V measurements were performed using a HP 4285A LCR meter. I-V measurements were carried out by Agilent 4156C semiconductor parameter analyzer.

3. Results and discussion

Fig. 1 shows the VLS growth mechanism of the nanowires. The gold nanoparticles have been used as the seed for the Ge nanowire growth. The size of the gold nanoparticels estimated from SEM image is around 20-40 nm (not shown here). Fig. 2 presents a FE-SEM image of Ge nanowires consisting of a dense mesh of long nanowires. The average diameter of the nanowires is 60-80 nm, whereas the length of the nanowires ranges up to few micrometers. EDS analysis (Fig. 3) confirms the Ge-NWs. To study the defects of the Ge-NWs, we have recorded photoluminescence (PL) spectra of the Ge-NWs (Fig. 4). The spectrum for the Ge nanowires has been decomposed into four component peaks using Gaussian fitting (Fig. 5). They are found to be centered mainly around 460 nm (2.7 eV), 476 nm (2.6 eV), 515 nm (2.4 eV) and a weak peak at 540 nm (2.3 eV). The origin of the PL peaks is attributed to oxygen vacancies V_o^-, oxygen-germanium vacancy pairs $(V_{Ge,}V_o)^+$ and related defect centers. The broad emission can be explained by a simple mechanism. The acceptors will be formed by $(V_{Ge,}V_o)^+$, and contributes to donors. After the excitation of carriers from impurities, a hole and an electron are created. Blue emission occurs when they recombine [4]. The schematic of the nanowire embedded MOS capacitor in an IrO_x/Al_2O_3/Ge-NW/p-Si structure has been shown in Fig. 6. The C–V hysteresis characteristics of the pure Al_2O_3 charge trapping layers (Fig. 7) and Ge nanowires embedded in Al_2O_3 layer (Fig. 8) are investigated. A small memory window of 1.2V under a sweeping gate voltage of ±7V is observed for pure Al_2O_3 charge trapping layers, while a large memory window of 3.9V is observed for Ge nanowire charge trapping memory capacitors with the same operating voltage. A large memory window of 3.1 V is also observed under a small sweeping gate voltage of ±5V. The memory window of Ge nanowire capacitor is higher than that of pure Al_2O_3 charge trapping layer (Fig. 9). It is suggesting that the extra charge trap on the Ge nanowire surface may be one of the possible reasons. The oxygen vacancy on the Ge nanowire surface can trap more holes rather than the electrons because of C-V shifted towards negative side. A moderate retention characteristic with a memory window of 0.9V after 2 hours elapsed time is observed (Fig. 10). It is very interesting to note that the resistive switching memory characteristics is observed for the same MOS structure with Ge nanowires (Fig. 11). The measurement of current-voltage (I-V) hysteresis is shown by arrows 1-4. A large SET and RESET voltages are found to be +5.1V and -4.0V, respectively. It is believed that the high resistance state (HRS) and low resistance state (LRS) are observed due to the oxygen vacancies on the Ge nanowire surface. The resistive memory device with a resistance ratio (HRS/LRS) of ~2 has a good data retention of 2000s (Fig. 12), which can be useful in future nanoscale nonvolatile memories.

4. Conclusions

In summary, the Ge nanowires have been prepared using VLS mechanism on Au-catalyzed Si substrates. A broad peak in photoluminescence spectrum between 350 to 500 nm is due to germanium-oxygen and oxygen vacancies. Good flash and resistive memory devices are obtained by using Ge nanowires MOS structure for the first time, which can be useful in future nanoscale memories.

Acknowledgments

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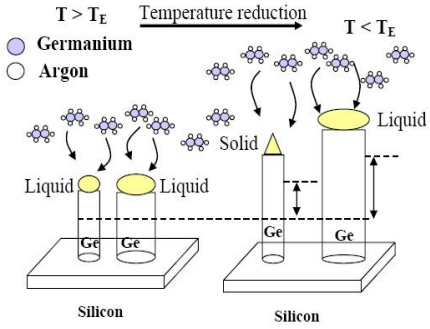

Fig. 1. Schematic of VLS growth mechanism for the Ge nanowires (Ge-NWs).

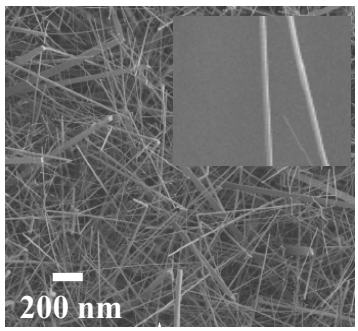

Fig. 2 Field emission scanning electron microscope (FE-SEM) image of VLS grown Ge nanowires. The high density Ge nanowires were observed by our growth process.

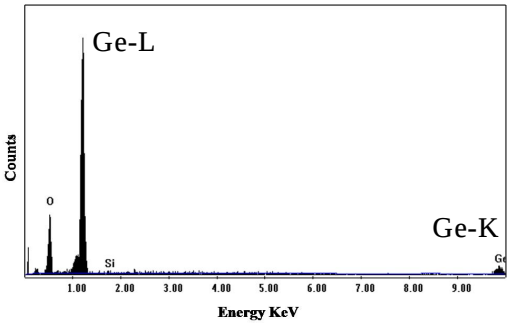

Fig. 3 Energy dispersion spectroscopy (EDS) analysis confirms the Ge nanowires.

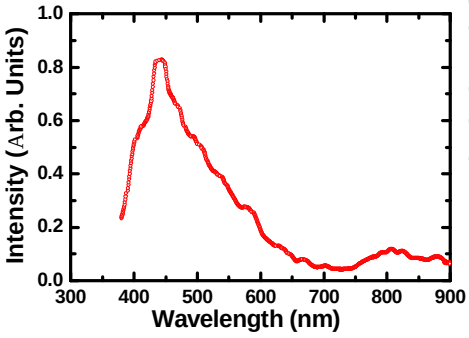

Fig. 4 Photoluminescence (PL) spectrum of the Ge nanowires after growth on Si substrate.

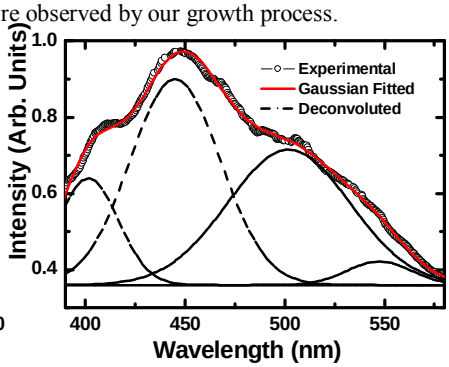

Fig. 5 Gaussian fitting of PL spectrum in the range of 375 nm to 600 nm for the Ge nanowires. Due to the surface defects (i.e. oxygen vacancies), the spectrum was broad.

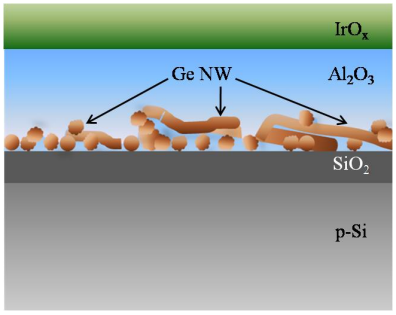

Fig. 6 Schematic of the nanowire embedded MOS capacitor device. The Ge-NWs were dispersed on the SiO_2 (5 nm)/p-Si substrate and fabricated the MOS diode structure.

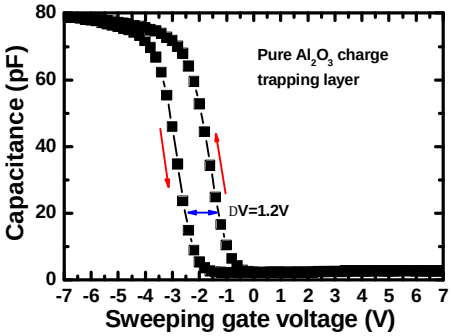

Fig. 7 High-frequency C-V hysteresis characteristics of a pure Al_2O_3 charge trapping layers. A small hysteresis memory window of 1V is observed.

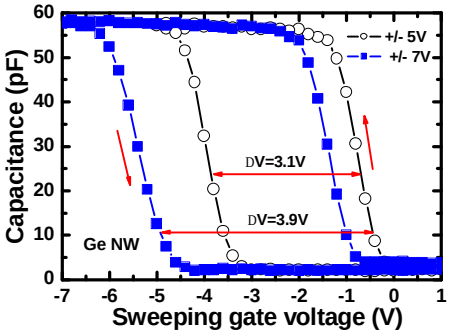

Fig. 8 Excellent C-V hysteresis characteristics of Ge-NW capacitor are observed, due to charge trapping on the Ge-NWs.

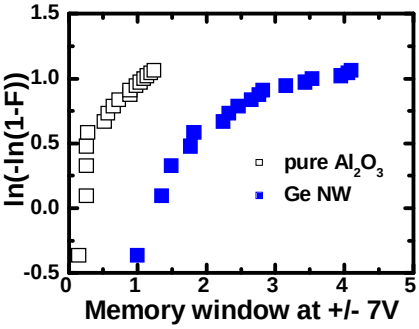

Fig. 9 Weibull plot of hysteresis memory window of pure Al_2O_3 charge trapping layers and Ge-NWs.

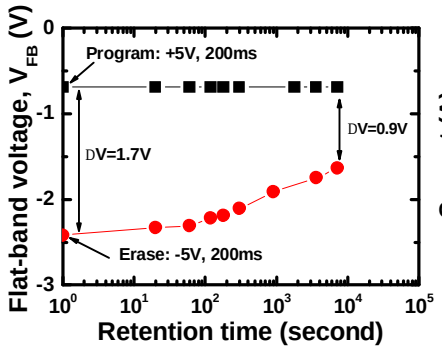

Fig. 10 Retention characteristics of Ge-NWs capacitors under a small program/erase voltage of 5V. A good memory window of 0.9V after 2 hours elapsed time and moderate charge loss of 50% are observed.

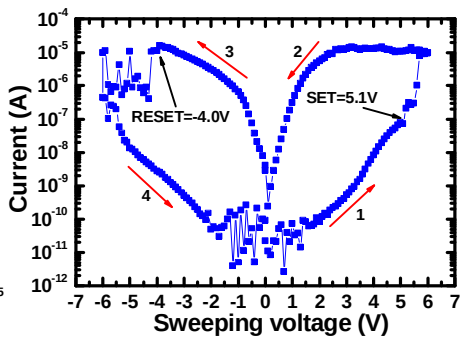

Fig. 11 I-V hysteresis characteristics of a Ge-NW MOS structure (IrO_x/Al_2O_3/Ge-NW/p-Si). The large SET and RESET voltages are observed and it could be modified by modifying the thickness of each layers.

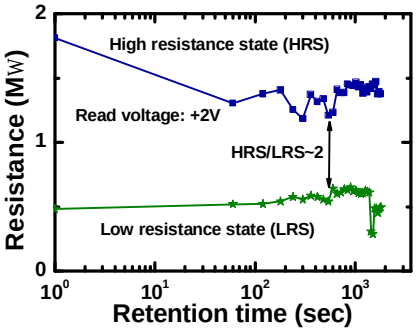

Fig. 12 Good retention characteristics of a Ge-NW MOS diode are observed. The read voltage was +2V. The resistance ratio (HRS/LRS) is about 2, which can be useful for nanoscale nonvolatile memory applications.