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Single Electron Transistors (SETs) for Reducing Source/Drain Resistance and MOS Current

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1. Introduction

Since a Metal-Oxide-Semiconductor (MOS) was developed, the scaling down of devices has been the most effective method for the improvement of device performance. However, as the scaling down of devices reaches sub-micron region, it reveals problems such as the short channel effect and power consumption.

Single-Electron-Transistors (SETs) which better operation with further scaling down are being studied, due to their many advantages. The SETs use only a few electrons and they offer low power consumption.

However, SETs have many advantages, there are still many drawbacks. Most of all, the operation temperature of SETs is too low. Also, For practical application, we need fabrication method to make a small Coulomb island reproducibly and controllably.

A Dual-Gate SET (DG-SET) make a small quantum dot by electrically formed tunneling barriers [1]-[3], and utilizes a relatively reproducible and controllable fabrication method.

In this paper, we fabricate dual-gate single-electron transistors (DG-SETs) having recessed structure and sidewall patterning with optimized parameters for room temperature operation.

2. Device structure and Fabrication

The device has a silicon nanowire channel and self-aligned gates. Fig. 1 shows a schematic of a SET with a sidewall gate on a nanowire. The Coulomb island in the nanowire is formed by the control gate, V_{CG}, and two tunnel junctions are formed by the sidewall gate voltages, V_{SG}. The potential of the electrically formed island is controlled by the control gate voltage, V_{CG}. Fig. 2 shows the proposed fabrication process flows. A schematic of SOI nanowire formation technology is shown in Fig. 2(a). This method enables a nanoscale patterning by using a combination of e-beam and photo lithography technology. In addition, Fig. 2(b) shows the process sequence for the formation of recessed channel and sidewall gates on nanowire.

The device was fabricated on SOI wafer. The active region was defined through a mix-and-match of photo and electron beam lithography. Then an SOI nanowire is formed after dry etch in Fig. 3(a). An SiO_2 layer is deposited through a plasma enhanced chemical vapor deposition (PECVD). The SiO_2 layer is patterned by e-beam lithography. After etching the patterned SiO_2 layer completely, the Si nanowire in the patterned region is partially etched to form a recessed channel in Fig. 3(b). Afterwards, control gate oxide is formed through thermal oxidation. This process helps reduce the dimensions of channel. Then, in order to form poly-Si sidewall spacers, poly-Si with n^+ doped layer is deposited and subsequently etched back to form the separated side gates. These formed sidewall spacers role as side gates and inter-gate oxide is grown by thermal oxidation process on the side gates.

Afterwards, a poly-Si layer is deposited using low pressure chemical vapor deposition (LPCVD) to form the control gate. In order to align the gate and the recessed channel, poly-Si layer is planarized by chemical mechanical polishing (CMP) process. After the poly-Si control gate is formed, the SiO_2 layer around the gate is removed. Subsequently, As^+ implantation is conducted to form the shallow junction region. The purpose of this is to form the extended channel of the device. Afterwards, the tetraethylorthosilicate (TEOS) oxide layer is deposited along the control gate and source/drain. The TEOS oxide is etched through a dry etcher. Then, TEOS oxide sidewall spacer is formed along the control gate in order to extend the channel. Finally, As^+ implantation is conducted to form the source/drain region in Fig. 2(b) and Fig. 3(c).

3. Results and Discussion

The overall fabrication process is highly compatible with the conventional CMOS process. Moreover, the process sequence is similar to virtual MOSFET [4].

In addition, making the integration of various CMOS-SET hybrid circuit applications that have previously been suggested is possible [3]. Fig. 4 (a) shows a room temperature transfer characteristics of the fabricated SET. From the transfer characteristics, it can be noted that the MOS current is much lower than that of previous DG-SET [4] from the grade (A) and (B) in Fig. 4 (B) . Also, as noted from Fig. 4 (b), the position of the Coulomb oscillation peak is controlled by V_{SG}, which is attributed to sharing of the island charge between the control gate and side gates.

4. Conclusion

We fabricate the newly proposed single electron transistor (SETs) with high process compatibility with

MOSFET and output characteristics of the devices are investigated for various bias conditions. The proposed structure has better performance in suppressing MOSFET current and reducing dimension of Coulomb island compared to previously presented structures. The device shows Coulomb oscillation at room temperature (300 K).

5. References

[1] D. H. Kim et al., IEEE Trans. Electron Devices, Vol **49**, no. 4. Pp. 627-635. 2002

[2] D. H. Kim et al., J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct., vol.**20**, no.4, pp. 1418-1418, 2002.

[3] S. Kang et al., Jpn. J. Appl. Phys., vol.**47**. no.4, pp.3118-3122, 2008

[4] W. Y. Choi et al., Jpn. J. Appl. Phys. **41** (2002) 2345.

Acknowledgements

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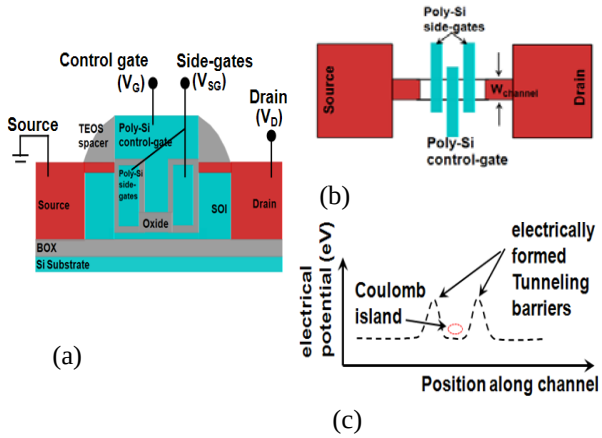

Fig. 1. Cross-sectional (a) and plain (b) views of the newly proposed device, and the potential profile along narrow channel (c).

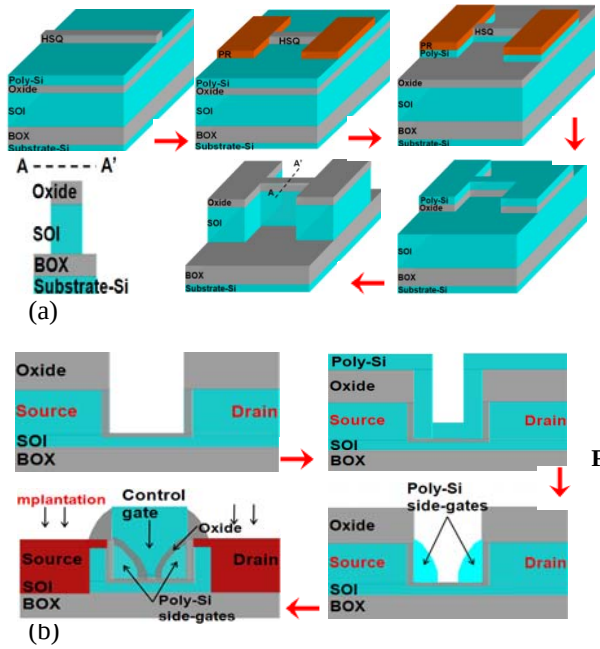

Fig. 2. Schematics of the process sequence of the nanowire patterning methods using the mix-and-match (a) and proposed fabrication process flows of the sidewall patterning technique (b).

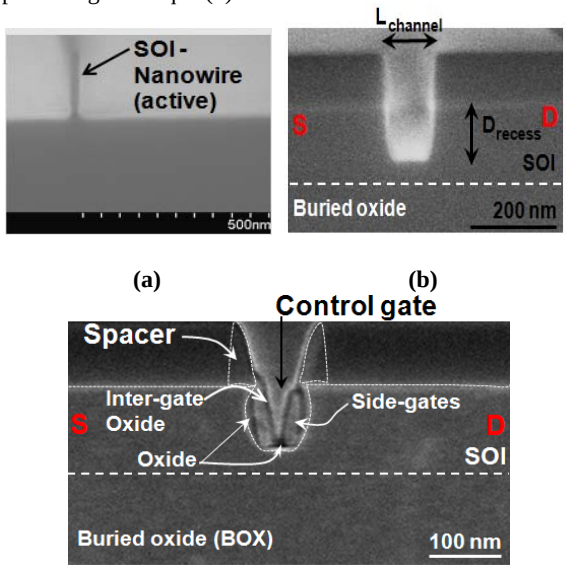

Fig. 3. SEM images of (a) a SOI nanowire, (b) recessed channel, and (c) poly-Si sidewall gates and control gate.

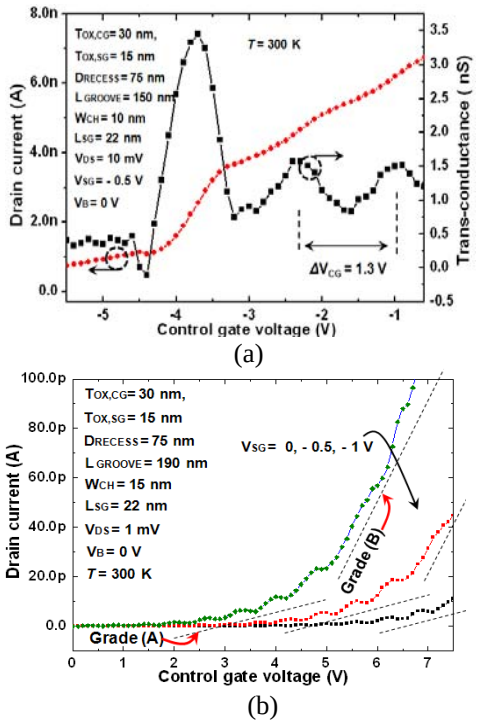

Fig. 4 I_{ds}-V_{cg} characteristics as a function of V_{CG} at room temperature of the fabricated device (a) and the Side-gates bias are 0, -0.5, - 1.0 V, respectively (b).