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Switching voltage reduction of resistance switching memory using $Si/CaF_2/CdF_2$ quantum-well structures

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1. Introduction

The dimension of the elements consisting integrated circuits is going down into nano-scale. One essential building block for nanoscale solid state devices is electric potential sequences for controlling electron transport, which can be implemented using energy band discontinuity at heterointerfaces. A $CdF_2/CaF_2/Si$ heterostructure is an attractive candidate for applications on Si substrates, such as resonant tunneling diodes (RTDs) [1] and coulomb blockade devices, because of the large conduction band discontinuity (ΔE_C~2.9eV) at the heterointerface [2] and small lattice mismatch with silicon. Due to the large ΔE_C, leakage current is expected to be suppressed in low level even at room temperature and moreover, voltage for tunneling transport can be reduced by utilizing multi-quantum-well tunneling scheme such as resonant tunneling or sequential tunneling with appropriate design of quantum-well layer thickness sequences. Up to now, we have demonstrated large peak-to-valley current ratio (PVCR) of CdF_2/CaF_2 RTDs larger than 10^5 at RT [3,4], which confirmed advantage of the large ΔE_C heterostructure material systems. And moreover, we have proposed and demonstrated novel scheme of resistance switching diode or resistance random access memory (ReRAM) using $Si/CaF_2/CdF_2/CaF_2/Si$ quantum-well (QW) structure [5]. In principle, low voltage write/erase and long retention time can be expected simultaneously under appropriate design because of the Si/CaF_2 double step energy barrier structures. In this study, we have demonstrated switching voltage reduction less than 1V by doping control of Si injector/barrier layer of the $Si/CaF_2/CdF_2/CaF_2/Si$ QW heterostructures.

2. Structure

Figure 1 shows schematic device structure and band diagram (flat band) proposed in this study. Basic concept of the device is $CaF_2/CdF_2/CaF_2$ double-barrier resonant tunneling diode structure or quantum-well (QW) structure sandwiched by silicon as the secondary energy barriers. CaF_2 layers act as energy barriers mainly for charge injection and ejection between a CdF_2 QW and a reservoir of electrons. Si layers act as energy barriers for suppression of electron escape from the CdF_2 QW. Using this layer configuration, write/erase voltage can be controlled in the range of 1 - 3 V by designing the appropriate thickness of CdF_2 quantum-well (2.5 nm-thick CdF_2 QW is one example) based on resonant tunneling scheme. Injected electrons are retained in CdF_2 QW because conduction band minimum of CdF_2 is ~0.6eV lower than that of Si therefore retention time can be controlled by the thickness of Si barrier layers. Figure 2 shows operation principle of the device. In writing operation, electrons are injected from an metal (Al) layer or n-type Si layer by resonant tunneling and a part of the electrons are trapped in CdF_2 QW as shown in (b). Injection from n-type Si layer is more preferable for low voltage switching operation. Trapped electrons are confined in CdF_2 QW by CaF_2 and Si energy barriers as shown in (c). In the result, resistance switching occur at around peak voltage of RTD. Resistance modulation (ON/OFF) ratio of more than 1000 can be expected theoretically due to the difference of tunneling probability between (b) and (c) under appropriate layer thickness configuration.

3. Fabrication

$Si/CaF_2/CdF_2/CaF_2/Si$ multilayered structures were grown in SiO_2 holes of 1μm-diameter formed on p-type Si(111) 0.1° off substrate. The hole arrays were prepared by using photolithography and wet chemical etching followed by SPM cleaning. Using molecular beam epitaxy (MBE) based technique, a 0.9-nm-thick CaF_2 layer was grown at 650°C. Subsequently, a 2.5-nm-thick CdF_2 quantum-well layer, 0.9-nm-thick CaF_2 layer were grown at 80°C and 40-nm-thick n-type Si layer were grown with As flux using valved cracking cell. After unloaded from the UHV chamber, Al/Au electrodes of 100 μm square were formed by lift-off.

4. Results and discussions

In the measurement of I-V curve shown in Fig. 3, bipolar resistance switching cycle has been clearly observed at room temperature, where switching voltage (low resistance state to high resistance state) was 1.0 V ("wri te" voltage) and peak-to-valley current ratio was around 25. Voltage for discharge or "erase" operation was found to be -1.8 V. Voltage for writing (V_{write}) has been dramatically decreased by n-type doping of the Si barrier layer, where V_{write} was 2.5 - 4 V for the device with non-doped Si layer of 1 nm-thick. Unipolar operation of the device will be also discussed.

5. Conclusion

We have proposed and demonstrated novel resistance switching diode using $Si/CaF_2/CdF_2/CaF_2/Si$ double heterostructure tunneling barriers and one quantum-well struc-

ture. Resistance switching voltage has been reduced less than 1V using doping control of a Si barrier layer, where 2.5 - 4V was required when using i-Si barrier layer.

Device concept proposed in this study is one possible candidate for new volatile memories or logic elements for future LSI technologies toward ultimate scaling in nanometer scale.

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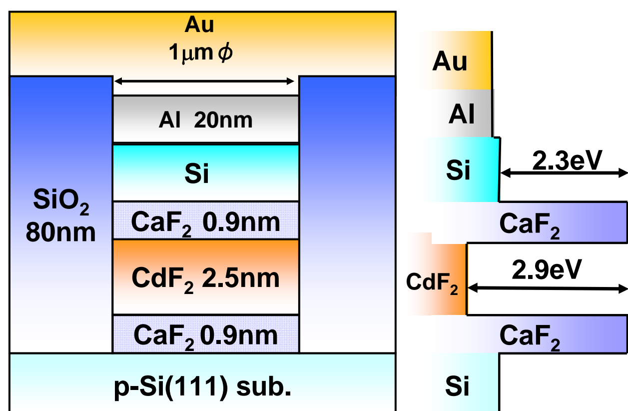

Fig.1 Schematic device structure and conduction band profile.

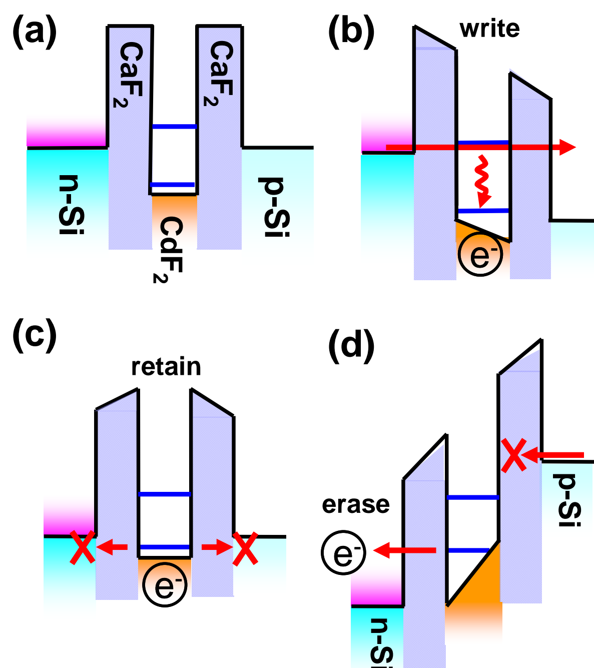

Fig.2 Band diagrams corresponding to (a) flat band potential, (b) "write", (c) "retain", (d) "erase" operation.

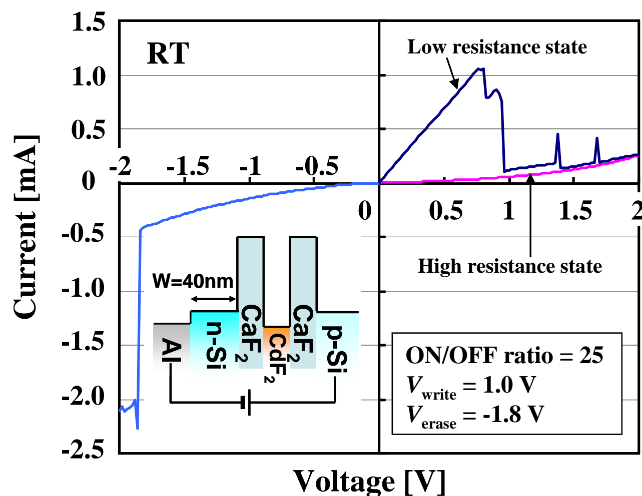

Fig.3 I-V curve at room temperature exhibiting bipolar resistance switching. Switching voltage for changing resistance from low resistance state into high resistance state has been observed at 1.0 V and ON/OFF ratio is around 25.