

# Time dependent analysis of the applied voltage operation for ensuring 10-year lifetime with SiN MOSFET noise source device

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## 1. Introduction

The increasing importance of high-quality random numbers reflects rising demand for network security systems. Embedded “physical” random number generators (RNG) are required for widely used SoC devices, since risks of the *side channel attacks* are increasing [1]. The need for a RNG capable of generating unpredictable random numbers has recently emerged. We have studied a physical RNG with SiN-MOSFET noise source devices (Fig.1). Structurally, the SiN-MOSFET RNG is similar to the MONOS memory device, and the different part is a very thin tunnel oxide layer (0.7nm), as shown in Fig.1. In accordance with electron injection/ejection in many local traps through the thin tunnel oxide, a large conductance change in the transistor naturally appears as a large  $I_D$  fluctuation. Using this device, we have realized a high generation rate RNG with a small circuit [2], as shown in Fig.1. However, ensuring long-term device reliability has been challenging as the MONOS memory, because the device has many local traps and electrons are injected/ejected frequently.

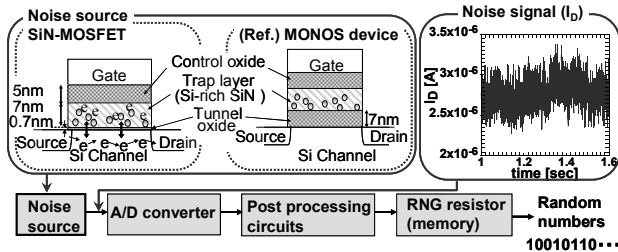
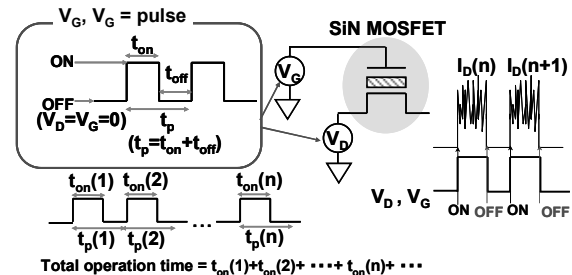


Fig.1 Concept and schematic of device structure.  
Gate length  $L=0.11\mu\text{m}$ , gate width  $W=0.18\mu\text{m}$ .

In this work, we have analyzed long-term change in device characteristics of the SiN MOSFET noise source from short-term experimental data and clarified how to ensure reliability over 10 years

## 2. Analysis of short-term measurement results

SiN-MOSFET with  $0.18\mu\text{m}$  channel width was fabricated based on 40 nm CMOS process. Figure 2 shows an overview of measurement conditions. It should be noted that ON-time,  $t_{on}$ , and OFF-time,  $t_{off}$ , (Fig.2) for applying voltage pulse to SiN-MOSFET can be more widely selected by changing usage conditions of RNG compared with MONOS memory. Typical  $t_{on}$  is one to several seconds and typical pulse time ( $=t_{on} + t_{off}$ ) is 5 to 100 sec. Figure 3 shows measurement results on  $I_D$  reduction as a function of total operation time for applying pulse with different pulse duty ratios. In each pulse duty ratio, although  $I_D$  decreases



$$\text{Total operation time} = t_{on(1)} + t_{on(2)} + \dots + t_{on(n)} + \dots$$

Fig.2 Overview of measurement conditions. The pulse time of  $V_D$  is synchronized with that of  $V_G$ .

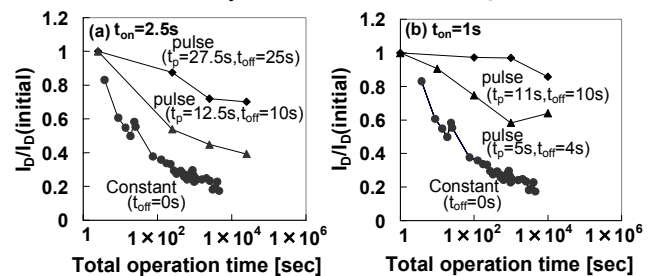


Fig.3 The Time dependent  $I_D$  for (a)  $t_{on}=2.5\text{s}$  and (b)  $t_{on}=1\text{s}$ .  
Longer  $t_{off}$  leads to gradual  $I_D$  reduction.  $V_D$  and  $V_G$  at on time are 1.5V and 2.5V, respectively.

with increasing total operation time, tunnel oxide breakdown was not observed in  $I_D$  characteristics. This indicates that as the OFF-time,  $t_{off}$ , increases the reduction rate of  $I_D$  decreases for the same total operation time. From the similarity to MONOS memory, it is thought that the origin of long-term change in  $I_D$  is gradual  $V_{th}$  shift caused by electrons trapped in deep level traps of SiN.

## 3. Long-term change in device characteristics

To preclude trapping of electrons at deep levels, the appropriate conditions for device operation should be clarified. We have compared these measurement results with similar characteristics of MONOS, where increase of traps in tunnel oxide layer shifts threshold voltage ( $V_{th}$ ) largely and, as a result, decreases  $I_D$  [3, 4]. Since  $I_D$  reduces logarithmically with  $V_{th}$  shift as the time based on a conventional MOSFET model, it has been found that  $I_D$  can be fitted by  $I_D/I_D(\text{initial})=a\{\log(t)\}+b$  with every  $t_{on}$ , where  $a$  and  $b$  are constant and the ideal  $a$  and  $b$  is 0 and 1, respectively. Figure 4 shows the fitting graphs of the reduction rate,  $b-I_D/I_D(\text{initial})$ , as a function of  $t_{off}/t_{on}$ . This result shows that shorter  $t_{on}$  leads to smaller  $I_D$  reduction for the same total operation time, even if the  $t_{off}/t_{on}$  is the same. By determining the parameters,  $a$  and  $b$ , by fitting experimental data to the above equations, it is possible to predict the  $I_D$  after 10 years under various usage conditions (under an

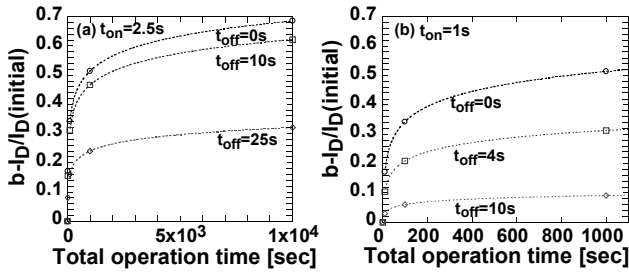


Fig.4 Approximate line  $I_D$  reduction rate in Fig.3 for (a)  $t_{on}=2.5s$  and (b)  $t_{on}=1s$ . Curve fit results of  $I_D$  in  $I_D/I_D(initial)=a\{\log(t)\}+b$  from each  $t_{on}$  and  $t_{off}$ .  $I_D$  reduction rate increase logarithmically.  $t$  is Total operation time.

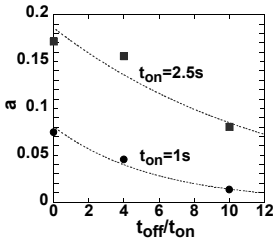


Fig.5 Period dependence of efficient "a." in Fig. 4.

operation time per day), as shown in Fig. 6 (a). Here,  $t_{on}$  is 1s or 2.5s, and the number of  $t_{on}$  pulse application per day,  $N_c$ , is 100 or 1000. (For example, in case of  $t_{on}=1s$  and  $N_c=100$ , total operation time per day is 100s.) When  $t_{on}=1s$ , the  $I_D/I_D(initial)$  did not reduce in each case, whereas, when  $t_{on}=2.5s$  and  $N_c=1000$ , there was a 35% decline in  $I_D/I_D(initial)$ . Fig.6 (b) shows  $I_D$  reduction rate after 10 years' usage versus  $N_c$ , which is estimated by Fig.6 (a). Since 10% reduction in  $I_D$  is acceptable considering the AD converter performance,  $t_{on}=2.5s$  and less than 1000 cycles/day are requirements for 10 years' reliability for the RNG.

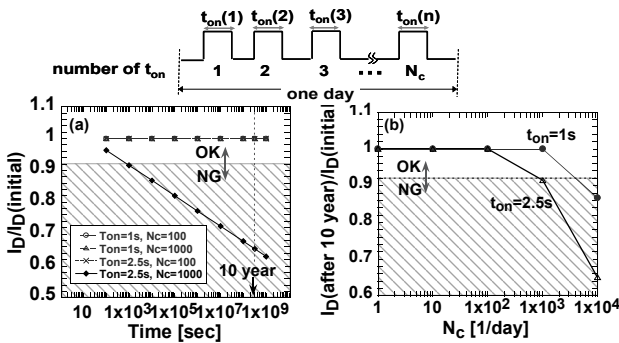


Fig.6 (a) Time dependent  $I_D$  reduction rate.  $I_D/I_D(initial)=a\{\log(t)\}+b=a\{\log(N_c n t_{on})\}+b$ , where  $n$  is number of days using the device. (b) cycle/day dependent  $I_D$  after 10 year ( $n=3650$ ) reduction rate.

#### 4. Influence of applying voltage on long-term change

$t$  has also been found that higher voltage leads to larger  $I_D$  reduction in  $I_D-V_G$  characteristics and lower voltage application is preferable(Fig. 7(a), (b)). This means that electrons easily trapped into deep level traps in SiN when high voltages are applied to the SiN-MOSFET, which is consistent with results of MONOS. Although the noise power decreases with decreasing applied voltages, it has been already confirmed that applied voltages ( $V_D=1.5V$ ,  $V_G=2.5V$ ) are acceptable for RNG performance [2].

#### 5. Usage conditions to reduce dispersions

In addition, we should consider the dispersion of device

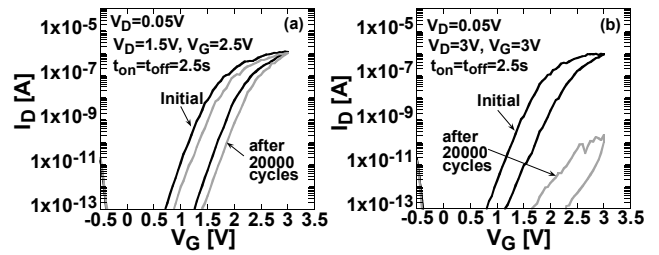


Fig.7  $I_D-V_G$  characteristics after applying 20000 cycles. (a)  $V_D=1.5V$ ,  $V_G=2.5V$ , (b)  $V_D=3V$ ,  $V_G=3V$ . Larger  $V_D$  and  $V_G$  lead to larger  $V_{th}$  shift.

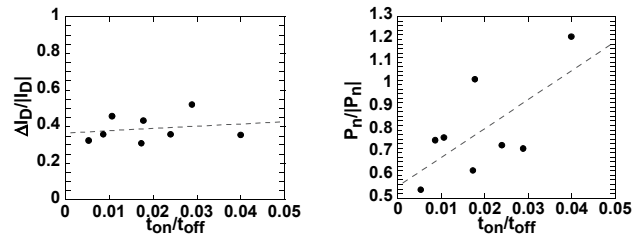


Fig.8 Dispersion of (a)  $I_D$  and (b) noise power  $P_n$  with  $t_{on}=1s$  to  $5s$ ,  $t_{off}=90s$  to  $300$ , shorter  $t_{on}$  leads to smaller dispersion.

characteristics so as to preclude electron trapping at deep energy levels. Figure 8 shows dispersion of  $I_D$  and noise power  $P_n$  versus pulse duty ratio. We clarified that the smaller pulse duty ratio leads to smaller dispersion of  $I_D$  and  $P_n$ . From the viewpoint of not only device lifetime but also dispersion, smaller duty ratio,  $t_{on}/t_{off}$ , is preferable for SiN-MOSFET based RNG.

#### 6. Conclusions: Conditions for long-term reliable SiN-MOSFET based RNG

We have theoretically evaluated long-term change in device characteristics of SiN MOSFET from device measurement data on short-term change. It has been found that, to improve the endurance, it is necessary to preclude electron trapping at deep levels by shortening  $t_{on}$ . Detailed conditions for 10 years' reliability are  $t_{on}<2.5s$ ,  $N_c<1000$  times,  $V_D=1.5V$ ,  $V_G=2.5V$ . For  $t_{on}=2.5s$ , 5M bit random-numbers (RNs) are generated per one cycle, since the generation rate of our RNG is 2Mb/s. These random-numbers are tentatively stored in resistors and used for CPU or security logics, as shown in Fig.9. For  $N_c=1000$ , 5G bit RNs are totally generated per day, which is sufficient volume for general usage of RNG.

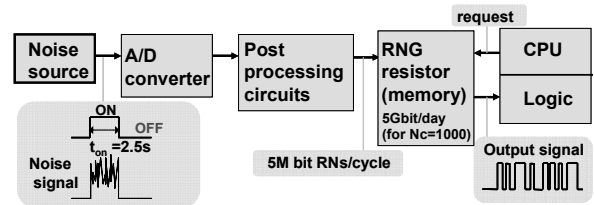


Fig.9 Concept for generating random numbers.

#### References

[1] P. Kocher et al., CRYPTO'99, (1999) 388  
 [2] M. Matsumoto et al., Jpn. J. Appl. Phys. **47** (2008) 6191.  
 [3] S. Minami et al., IEEE trans. Electron Devices **40** (1993) 2011  
 [4] G. Giusti et al., J. Appl. Phys. **106** (2009) 104506