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Three-Terminal Spin-Momentum-Transfer Magnetic Memory Element

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1. Introduction

Spin-momentum-transfer (SMT) magnetoresistive random access memory (MRAM) has received a good deal of attention recently because of its potential as a nonvolatile memory with good speed, density, endurance, and scaling attributes. Conventional two-terminal SMT MRAM offers simple fabrication and very dense structures, but will require substantial materials development for it to satisfy all attributes simultaneously.[1] One can ease demands on materials by separating the reading and writing functions of the device with the addition of a third terminal. For a modest cost in complexity and device size, one can more readily realize a structure that can simultaneously operate at high speed, high operating temperature, and with essentially infinite endurance.[2]

2. Embedded 3-terminal SMT MRAM

Motivation

Table I compares various types of memories with specifics tailored for embedded applications. Here we consider embedded memories because of the focus on performance rather than density and cost. For embedded SMT (eSMT) memories in particular, higher speed and higher thermal stability imply higher write current, but in 2-terminal devices, higher write current is more likely to cause magnetic tunnel junction (MTJ) barrier breakdown. By removing the MTJ barrier from the write current path, one could drive high write currents without concern for breakdown of the MTJ barrier.

Device Structure and Operation

The 3-terminal device structure used in this work is illustrated in Fig. 1. Write current entering the device through terminal T1 is shunted through a high conductivity nonmagnetic layer to terminal(s) T3 without traversing the MTJ barrier. A thin polarizing magnet between T1 and the shunt layer preferentially directs the electron spins, creating a spin accumulation region directly above T1. The spin accumulation region imparts torque on the free layer magnetization and may induce switching. With no need to pass high write currents, the MTJ barrier can be designed with a relatively high impedance for optimal magnetoresistance (MR).

The advantage of this type of structure is represented schematically in Fig. 2. In the 2-terminal device structure, device distributions within an array must concurrently satisfy the need for read voltage to be less than the voltage at which the device switches, the write voltage to be greater than the current at which the device switches, and the breakdown voltage to be greater than the write voltage. If these distributions overlap (as in Fig. 2A), the operation will fail. The 3-terminal device separates the functions so that one may separately optimize the read voltage with respect to the breakdown voltage and the write voltage with respect to the switching voltage.

Device Fabrication

The device illustrated at the top of Fig. 1 includes a redundant T3 terminal, and may be substantially shrunk for improved circuit density. The terminals T1 and T3 connect to the bottom polarizer layer with single-Damascene TaN vias 200nm in diameter. The magnetic stack is deposited without breaking vacuum including a seed layer, PtMn-pinned CoFe polarizing layer, a Cu(3% N) normal metal shunt – with nitrogen added for improved smoothness, CoFeB free layer, MgO tunnel barrier, and a CoFe / Ru / CoFe synthetic antiferromagnet reference layer pinned by a PtMn layer. MTJ shapes are etched to a depth just through the free layer using a combination of reactive ion etch (RIE) and ion beam etch

Table I Comparison of Embedded Memories (eMemories) at the 90nm Node

	eSRAM	eDRAM	eFlash	eFeRAM	ePCM	eField MRAM	eSMT MRAM	e3T-SMT MRAM
Size (cell area per bit, F^2)	140	25	~ 20	15	15	40	25	40
Cost (add'l masks)	0	5 – 9	7 – 11	2	4	3	1 – 2	2 – 3
Read Speed (ns)	1	2	60	40	15	15	30	< 5
Write Speed (ns)	1	2	8,000	80	200	30	30	< 5
Operating Temp. (°C)	≥ 120	≥ 85	≥ 100	≥ 125	70	≥ 105	≥ 125	≥ 125
Write Endurance (cycles)	$>10^{16}$	$>10^{16}$	~ 10^5	10^{10}	~ 10^8	$>10^{16}$	$>10^{16}$?	$>10^{16}$

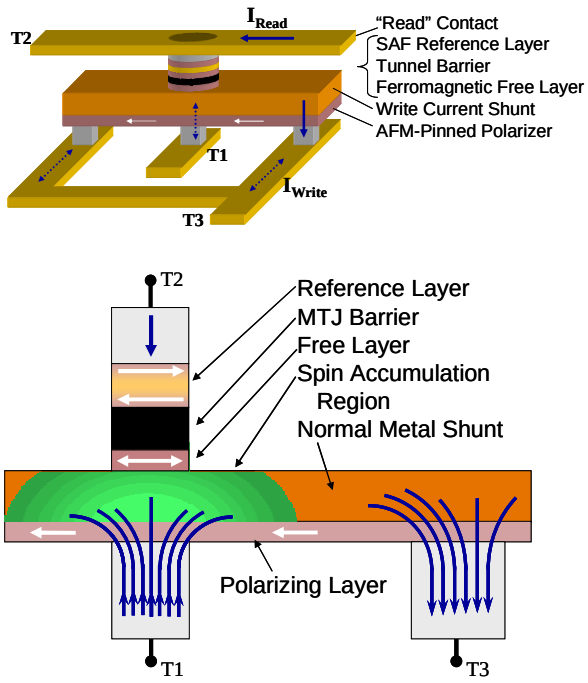

Fig. 1 3-Terminal device structure perspective (top) and partial cross-section (bottom) views. Dark arrows correspond to read and write currents. White arrows indicate magnetization direction. The write current is shown flowing between T1 and T3 terminals, whereas the much smaller read current flows between T2 and T3.

(IBE) techniques. The write current shunt layer is then defined with RIE and IBE, using a dielectric hard mask. Self-aligned top contact to the MTJ read element is made with dual-Damascene copper wiring in a planarized dielectric. A TEM image of the center of a representative device is shown in Fig. 3.

3. Results and Conclusions

Successful operation of these devices has been demonstrated with switching as fast as 1ns. Switching current of roughly 7mA was needed to switch in 1ns a device with thermal energy barrier of 39 kT (see Fig. 4). A similar device with energy barrier 64 kT required roughly 14mA to switch at 1ns. These devices showed expected robustness without MTJ barrier breakdown during the high-current switching tests. Work is continuing with investigation of perpendicular anisotropy magnetics in an effort to reduce switching current by a factor of 10.

Acknowledgements

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References

[1] R. Takemura et al., IEEE J. Sol. St. Circuits **45** (2010) 869.

[2] J.Z. Sun et al., Appl. Phys. Lett. **95** (2009) 083506.

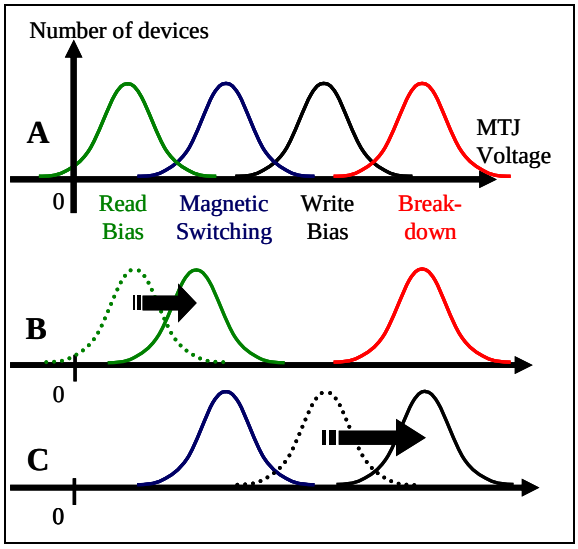

Fig. 2 Improvement of operating margins by separating the 2-terminal SMT operations (A) into separate read (B) and write (C) functions with 3-terminal SMT devices.

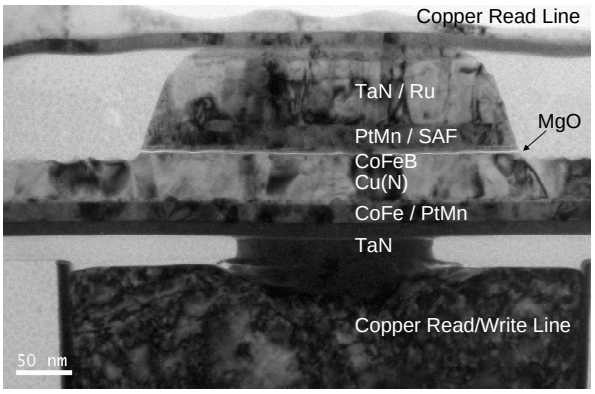

Fig. 3 TEM image of the central portion of a 3 terminal SMT MRAM device.

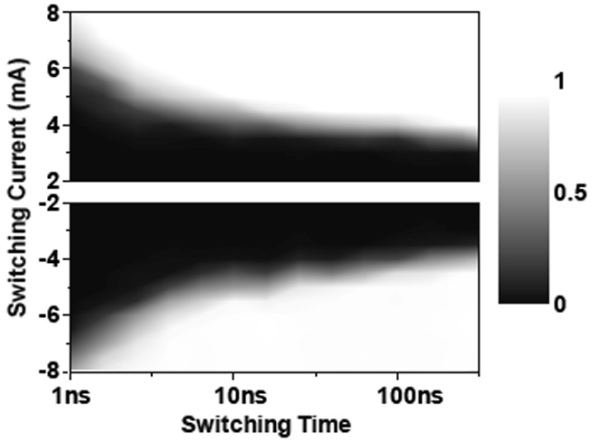

Fig. 4 Switching probability map for a roughly 100 x 150nm device with thermal energy barrier of 39 kT.