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Design of a Process-Variation-Aware Nonvolatile MTJ-Based Lookup-Table Circuit

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1. Introduction

The increasing demand for implementing nonvolatile field-programmable gate arrays (FPGAs) [1], [2] has been growing up for completely eliminating drastic increase of static power dissipation due to leakage current [3] with instant-on capability. As a promising solution, a nonvolatile lookup table (LUT) circuit using magnetic tunnel junction (MTJ) devices combined with MOS transistors, has been presented as a key component for the nonvolatile FPGA and the basic behavior using fabricated test chip is confirmed [4]. In order to implement the large-scaled nonvolatile FPGA, it is necessary that MOS/MTJ hybrid LUT circuit has robustness against process variation of MTJ devices which affects device characteristics such as resistance value and tunnel magneto-resistance (TMR) ratio [5].

This paper presents a process variation-aware LUT circuit using MOS/MTJ hybrid structure. Since switching operation is performed by the difference of the current value between LUT tree and the reference resistor tree, programmability of reference current level enables adjustment of threshold level according to the current value variation of the LUT tree. This programmability of reference current level is realized by utilizing series/parallel connection of redundant MTJ devices. Since MTJ devices are distributed sparsely on the LUT circuit plane, these redundant MTJ devices not affect the area of the LUT circuit. Moreover, variation compensation state can be retained in those MTJ devices with no power supply.

2. Process-Variation-Aware MTJ-Based LUT Circuit Structure

Fig. 1 (a) shows the symbol of an MTJ device. According to the spin direction of the free layer with respect to that of the fixed layer, the resistance of the device shows two distinct states; a low-resistance (R_P) state (when the spin directions are parallel) and a high-resistance (R_{AP}) state (when anti-parallel), and TMR ratio is defined as $\Delta R = (R_{AP}-R_P)/R_P$. Fig. 1 (b) shows the *R-I* characteristic of an MTJ device; when the current $I_{AP\rightarrow P}$ is applied to the MTJ device flowing from the free layer to the fixed layer, the resistance value of the MTJ device becomes R_P. In contrast, when the current $I_{P\rightarrow AP}$ in the opposite direction is applied, the resistance value of MTJ device becomes R_{AP}.

Fig. 2 shows a circuit diagram of the proposed MTJ-based 2-input LUT circuit(it can be easily extended to a 4-input one). The circuit is composed of a configurable logic circuit (CLC) by MTJ/nMOS network and a sense amplifier by pMOS network. Each of networks is implemented based on differential current-mode logic with dynamic power management [6]. A truth table for a 2-input logic function is stored in 4 MTJ devices at the bottom of a LUT tree in the CLC. The LUT tree determines a current path according to the input data (X_0, X_1) and generates a current I_F, while a programmable reference resistor tree generates a constant reference current I_{REF}. By comparing these two current values, voltages of the two output nodes (Z, $\overline{Z}$) are determined. This means that the operation margin of proposed LUT circuit depends on the difference between I_F and I_{REF}. Thus programmability of I_{REF} allows the capability of variation compensation.

Fig. 3 shows the circuit diagram of a programmable reference resistor. Programmability of reference resistance is realized by series/parallel connection of 4 MTJ devices. When ENB signal becomes high, nMOS transistors M_5, M_6 and M_7 turn on and the reference current path is activated. I_{REF} is determined by total resistance of MTJ devices and on-state resistance of nMOS transistors M_5, M_6 and M_7 and configuration of MTJ devices is performed by using individual current flow path, which is controlled by the word lines, WL_0, WL_1, WL_2, WL_3 and WL_4, and bit lines, BL_0, BL_1 and BL_2 (BL_0 and BL_2 are shared with CLC).

3. Evaluation

In this evaluation, we assume that the variations of R_P and ΔR are follow normal distribution and their normal deviations are expressed as σR_P and $\sigma \Delta R$. Fig. 4 (a) shows a monte-calro simulation result of conventional MTJ-based 2-input LUT circuit under the condition of σ=0.075; some errors are caused due to the variations of R_P and ΔR. On the other hand, Fig. 5 (b) shows a monte-calro simulation result of proposed 2-input LUT circuit under the same condition of conventional one; since I_{REF} is programmed to the most appropriate value according to the variations of R_P and ΔR, no error is caused. Fig. 5 shows the relationship between the probability of errors (P_{ERROR}) and the value of σ; P_{ERROR} of proposed circuit is reduced by 60% compared with conventional one when σ=0.15, moreover, it becomes almost zero when σ<0.10. Table 1 summarizes performance comparisons between a conventional 4-input LUT circuit and the proposed one. Although there is an area overhead of write access transistors, proposed circuitry does not affect the delay and active power.

4. Conclusions

In this paper, we presented a variation-aware nonvolatile LUT circuit. Series/parallel connection of MTJ devices enables programmability of reference current. As a result, operation errors are eliminated under σ<0.10. In future, the more write current of an MTJ device will be reduced, the smaller, the area overhead of write access transistors will become.

Acknowledgements

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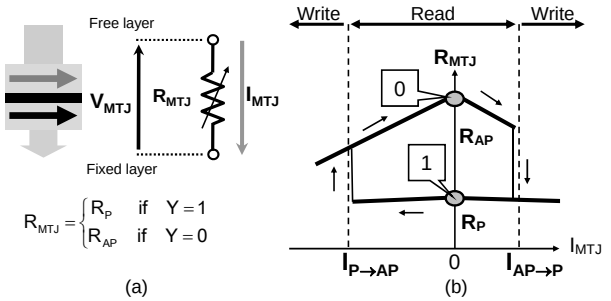


Fig. 1: Feature of MTJ device; (a) symbol, (b) *R-I* characteristic.

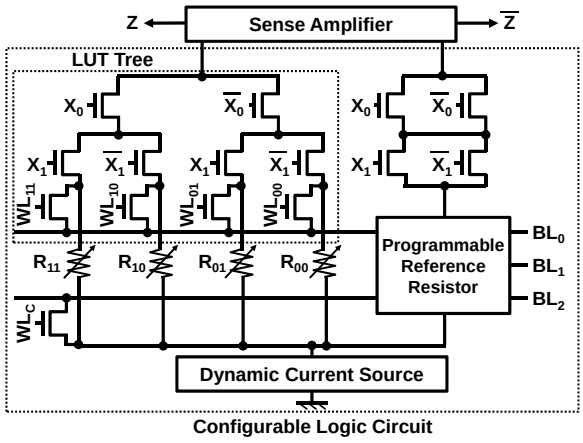
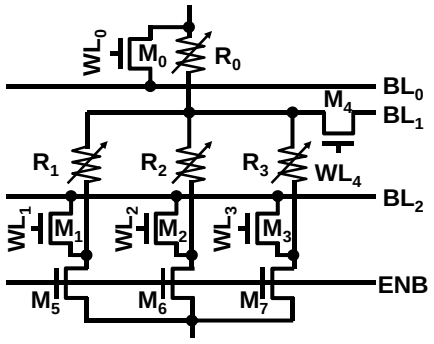


Fig. 2: Circuit diagram of proposed MOS/MTJ hybrid 2-input LUT circuit.



R_{ON} : On-state resistance of M_5, M_6 and M_7

Fig. 3: Circuit diagram of programmable reference resistor.

References

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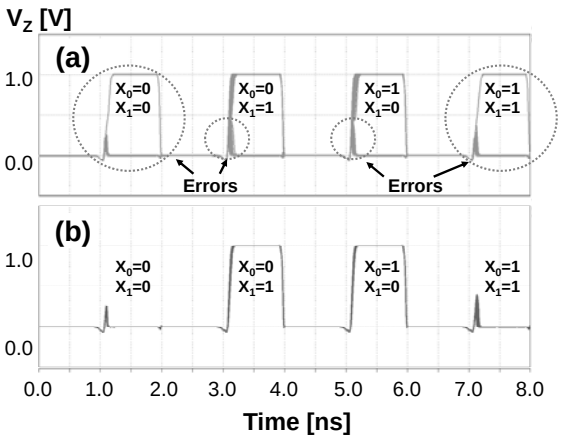
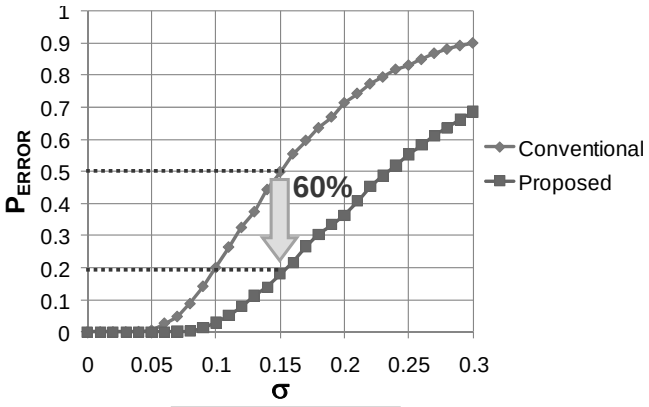


R_P = 2kΩ, ΔR = 1, σ = 0.075
HSPICE simulation under a 90nm CMOS technology.

Fig. 3: Output waveforms of XOR operation with variation; (a) conventional, (b) proposed.



R_P = 2kΩ, ΔR = 1

Fig. 4: Relationship between probability of error (P_{ERROR}) and variation (σ).

Table 1 Performance comparisons.

	Conventional	**Proposed**
Device Counts	69Tr.+16MTJ +1R	**77Tr.+20MTJ**
Active Power @250MHz	39.8uW	**39.8 uW**
Delay	0.46ns	**0.47ns**
Programmability of R_{REF}	No	**Yes**

R_P = 2kΩ, ΔR = 1
HSPICE simulation under a 90nm CMOS technology.