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RF Signal Generator Based on Time-to-Analog Converter Using Multi-Ring Oscillators in 90nm CMOS

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1. Introduction

Chip area reduction is essential of CMOS technology scaling, because device scaling has been able to give the low cost with low power and high speed, *i.e.*, ***the scalability***. However, the device scaling has not been of benefit to RF CMOS circuits effectively because the conventional analog circuits requires the use of unscalable components such as inductors and capacitors, resulting in the prevention of chip area reduction and wideband operation for multiband application. Furthermore, low-voltage operation has brought the difficulty of analog performance improvement. Recently, novel approaches of digital-rich and digitally controllable RF circuit techniques have been proposed [1-3]. However, the fine resolution for high signal-to-noise ratio requires the complicated circuit, resulting in the difficulty of chip area reduction.

In this paper, we propose a scalable wideband RF signal generator that uses a time-to-analog conversion technique using multi-ring oscillators, and discuss the fabricated 90nm CMOS circuit performance..

2. Time-to-Analog Converter

Conventionally digital-to-analog converters (DACs) generate analog signals. RF signal generation is considered to require the use of high-speed and high-resolution DACs. In order to obtain RF signals with low distortion of over 50 dBc, the 10-bit resolution is required [1]. However, the DACs are not suitable for low-voltage operation, because the required voltage-step becomes smaller in miniaturized and low-voltage CMOS. Therefore, we have investigated time-domain control, leading to voltage output using time-step control instead of the ordinary voltage-step control at regular time intervals and high resolution of time-domain to obtain high frequency, low distortion and high signal-to-noise ratio. Since the time-domain resolution is expected to be improved with miniaturization, the circuit is fundamentally scalable and could become wideband.

Figure 1 shows a block diagram of the proposed RF signal generator. A multi-tap fine delay circuit consists of delay elements using a ring oscillator to improve fine time resolution instead of two inverters [3]. The delay of two inverters was about 70 ps in 0.18μm CMOS process. The waveform digital controller controls the AND circuits. In the summing circuit, AND circuits are used for selection of delayed pulse signals. Delayed pulse signals of the ring oscillator could be consisted of four outputs of π/4 phase difference. By summing the delayed pulse signals, a desired RF signal could be synthesized. When delayed output signals from all the delay elements are selected, a triangular waveform could be synthesized from a rectangular input signal. A sinusoidal RF signal can be obtained by delayed signal tap selected from the following equation.

$$t_s(n) = \left[\sin^{-1}\left(\frac{y_s \cdot n}{A} \right) \right] \cdot \frac{1}{2\pi f} \quad , \qquad (1)$$

where $t_s(n)$ is the time value, A the amplitude of the sinusoidal signal, ys the voltage step, and f the frequency of the sinusoidal signal.

3. Chip design

A test chip was designed and fabricated using a 90nm CMOS process. Figure 2 is a block diagram of the whole RF signal generator using four voltage-controlled oscillators based on ring oscillators (ring VCOs) and three inverters between the ring VCOs as shown in Fig. 3. The delay τ is delay time of the delay element. The delayed pulse signals of the ring VCO could be consisted of each four outputs of π/4 phase difference selected by AND circuits. The number of all delay pulse signals is 16 (4-bit). To generate a sinusoidal RF signal, 14 delayed pulse signals are selected. The delay time of the three inverters and the frequency of the ring VCOs can be controlled by pMOS voltage shift. The delay τ is supposed to be 8.4 ps at 3.7 GHz. The circuit is also designed to be possible to suppress any harmonics by the three inverters. The delay time of the three inverters is controlled to suppress third harmonics. In the chips, the waveform digital controller circuit was omitted for convenience of evaluation. A chip photo-micrograph is shown in Fig. 4. The core size of the chip is 0.82 mm × 0.70 mm.

4. Measurement results

Frequency tuning range of ring VCOs was from 1.1 GHz to 3.7 GHz. The power supply is 1.0 V. Fig. 5(a) shows the measured output spectrum at 1.1GHz. The output signal level was −1.0 dBm and the third harmonic was −51.4 dBc. Fig. 5(b) shows the measured output spectrum at 3.7 GHz. The output signal level was −5.2 dBm and the third harmonic was −53.2 dBc. Both the output waveforms were shown in Fig. 6. Performances of the chip are summarized in Table I. Emphasis is that the third harmonics suppression was found to be more than 50 dBc using 14 delayed signals and this superior suppression was obtained by the delayed signals of less than 16 (4-bit). Furthermore, it should be noted that the selection of ring VCO outputs and the control of inverter delay times among VCOs can reduce any harmonics.

5. Conclusion

We have designed and evaluated an 1.1-3.7GHz signal generator using the time-to-analog conversion technique. Less than 4-bit resolution in time domain has enabled more than 50-dBc third harmonics suppression. The feature of circuit implementation is that circuit can consist of active devices, *i.e.* the circuit has ***the scalability***.

Acknowledgements

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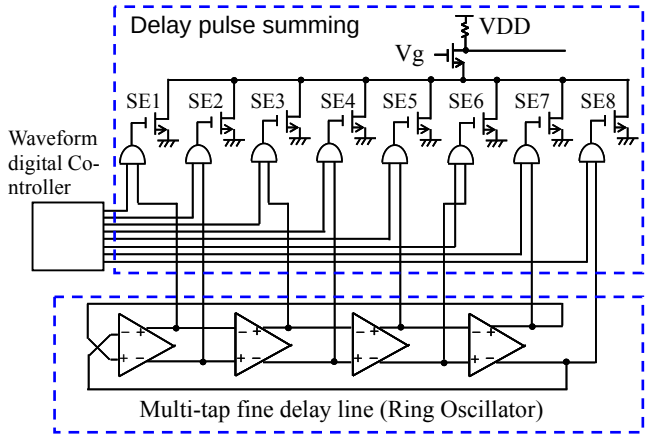

Fig.1 Block diagram of the RF Signal Generator

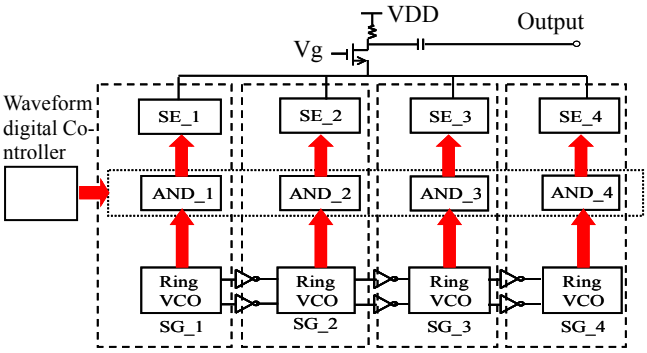

Fig.2 Block diagram of the whole RF Signal Generator

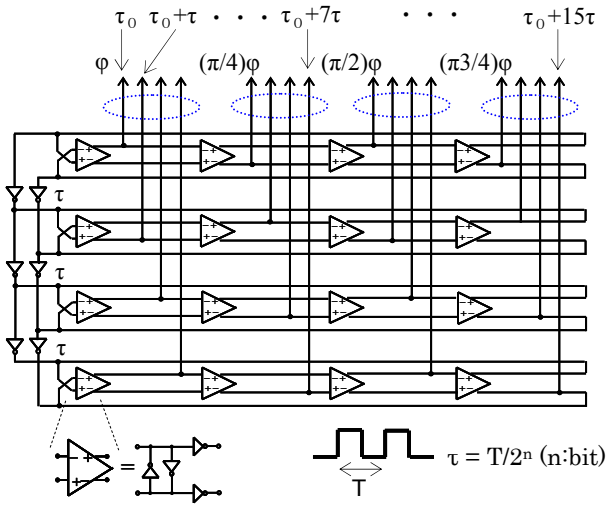

Fig.3 Block diagram of the ring VCOs
(Each four output selects : Total 16 selects)

References

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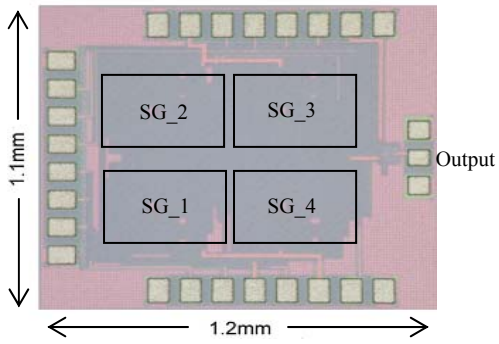
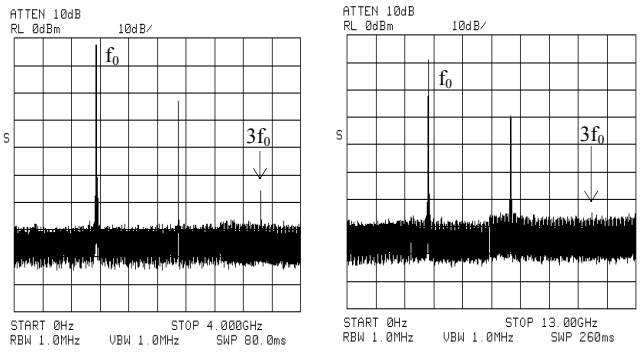
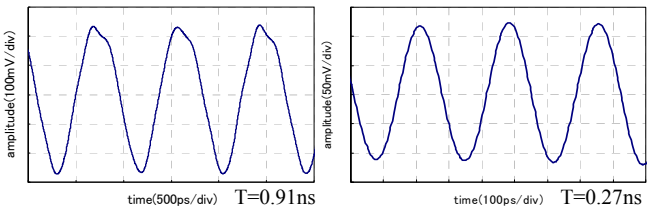


Fig.4 Chip micrograph of the RF Signal Generator



(a) (b)

Fig.5 Measured output spectrum with the harmonics
(a)f_0=1.1GHz (b)f_0=3.7GHz



(a) (b)

Fig.6 Measured output waveform
(a) f_0=1.1GHz (Period T=0.91ns) (b) f_0=3.7GHz (T=0.27ns)

Table I Performance summary

	This work	
CMOS Process [nm]	90	
Resolution	14 steps	
Frequency Tuning Range [GHz]	1.1 – 3.7	
Carrier frequency [GHz]	1.1	3.7
Output power [dBm]	–1.0	–5.2
Second harmonics [dBc]	–19.9	–20.1
Third harmonics [dBc]	–51.4	–53.2