

Confocal Imaging System Using 28.2 GSample/s UWB Sampling Circuit

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1. Introduction

Impulse radio ultra-wideband (IR-UWB) CMOS circuits have been developed for radar and imaging applications. A confocal imaging technique was presented for detecting a target which is surrounded by dielectric material using Gaussian monocycle pulse (GMP) [1][2]. By measuring the delay time between the transmitting and the receiving wave, the system can calculate the lengths of propagation paths. By the confocal imaging technique, the image of the embedded dielectric target can be reconstructed. For the accurate measurement of the delay time, a sampling circuit with the higher sampling rate is required.

In this paper, we adopt the 28.2 GSample/s equivalent time sampling (ETS) circuit with an improved multiplexer to a confocal imaging system.

2. System Design

System Configuration

The total system of the proposed detection system is shown in Fig. 1. It consists of transmitter (TX) and receiver (RX) circuits including a proposed sampling circuit. Both circuits are synchronized by the external oscillator clock. The transmitted signal by a TX antenna is reflected by a target and received by a RX antenna. To measure the delay time exactly, the sampling rate is an important factor of the sampling circuit. To realize such a high sampling rate, the ETS technique is adopted [3].

The sampling clock generator, shown in Fig. 2(a), is a key component to realize the high sampling rate. It consists of 4 blocks such as a phase locked loop (PLL) with a 1.76 GHz 8-stage ring voltage controlled oscillator, a multiplexer (MUX), a 16:1 frequency divider (DIV) and a delay circuit. Among the 16-phase PLL outputs, one signal is selected by the 16-to-1 MUX to determine the sampling timing. For accurate sampling, the transfer time between selected input node of MUX and the output node should be the same. In this circuit, MUX is composed of 8 2-to-1 MUX. In conventional 2-to-1 MUX (Fig. 2 (b)), a degradation of output signal occurs due to the charge transfer which is generated by the un-selected input signal. To reduce the effect, the switched cascade topology, shown in Fig. 2 (c), is adopted. The phase error of MUX is shown in Fig. 2(d), which is calculated by the difference between the transfer times of one selected input and the other. The error was reduced from 28.8 psec to 7.9 psec compared with the conventional MUX. After the MUX, the frequency of the timing clock is reduced to 110 MHz by the DIV. Accordingly,

110 MHz and 35.51 psec interval clock signals are formed. The signal is converted to 3 phase signal and sent to the track-and-hold (T/H) circuit and the analog-to-digital converter (ADC).

The ADC with the T/H circuit, shown in Fig. 3(a), converts a UWB signal to digital signal. Expanding the input bandwidth, the T/H circuit is adapted before the conventional 4-bit flash ADC which has 15 inverter type comparators shown in Fig 3 (c) [4]. In the proposed sampling

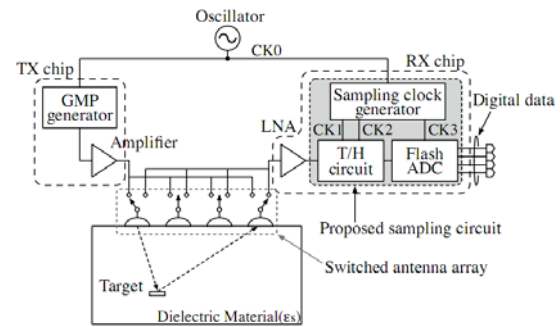


Fig. 1 Proposed imaging system.

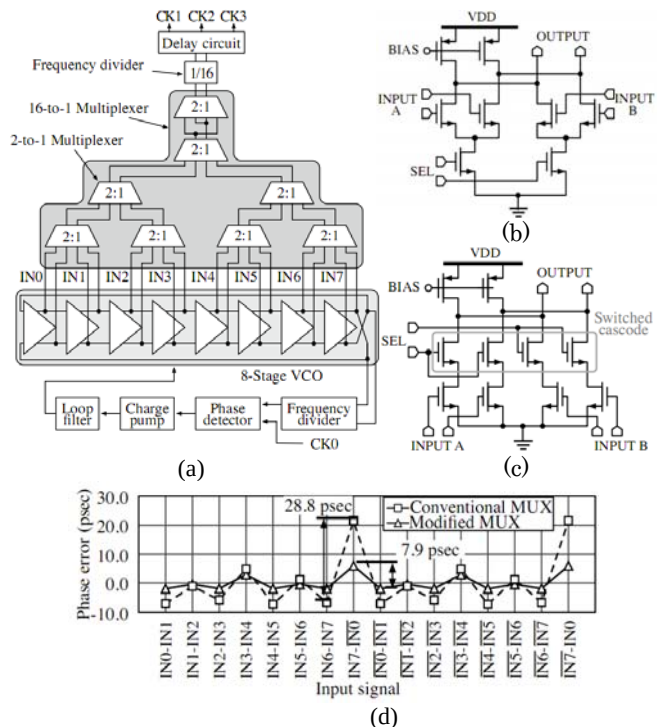


Fig. 2 (a) Sampling clock generator. (b) Conventional 2-to-1 MUX. (c) Improved 2-to-1 MUX. (d) Phase error on the conventional and the improved MUX (simulation).

circuit, the T/H circuit has a function to reduce the bandwidth of the GMP input signal to 110 MHz. To reduce the effect of charge injection, the series type T/H circuit, shown in Fig. 3 (b), is adopted. The downconverted signal (V_{LF}) is input to the ADC and converted to digital signals. For the error correction, the output digital signal through the error correct and the averaging circuit. As a result, the frequency of the output signal is reduced to 1/8192.

3. Measurement Results

The measurement setup with the proposed circuit and the chip and antenna photographs of the proposed system are shown in Figs. 4, 5 and 6, respectively. The transmitting signal is GMP with 3 GHz center frequency, shown in Fig. 7, and the sampling circuit detects the received signal. To transmit and received UWB signal, a 1.54 - 4.73 GHz bandwidth UWB slot antenna, shown in Fig. 6, and 1-30 GHz bandwidth GaAs amplifiers are used. To confirm the input waveform of the sampling circuit, the received waveform is separated by a hybrid coupler. After separating, one of the separated signals is input to the sampling circuit and the output is measured by oscilloscope A. Another signal is directly connected to oscilloscope B to measure the input signal of the sampling circuit. The specification of the proposed system is shown in Table 1. Using this system, a 6 cm square aluminum target which is placed 40 cm below antennas and the distance between the antennas is 20 cm. Figures 8 (a) and (b) show the input and the output signals of the proposed sampling circuit when the center of the antennas is placed above the target. There are reflected waves from the target and a direct wave from the transmitter. The position of antenna is relatively moved by 10 cm to the horizontal direction and the sampled waveform is measured. From these waveforms, the confocal image is constructed as shown in Fig. 8 (c). As a result, the detected signal can be applied to confocal imaging system, which is developed by use of CMOS circuits for the first time.

4. Conclusion

The detection system with 3 GHz center frequency GMPs was developed with the ETS circuits using 65nm CMOS technology. The sampling circuit is confirmed to detect the received signal and the confocal imaging system can detect the 6 cm Al target.

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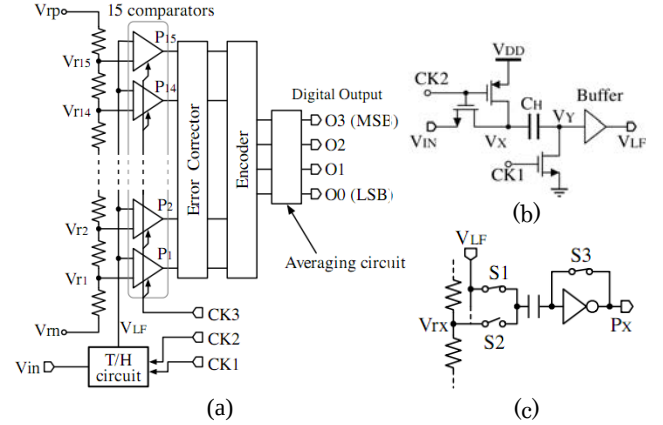


Fig. 3 (a) Wideband ADC. (b) T/H circuit. (c) Comparator.

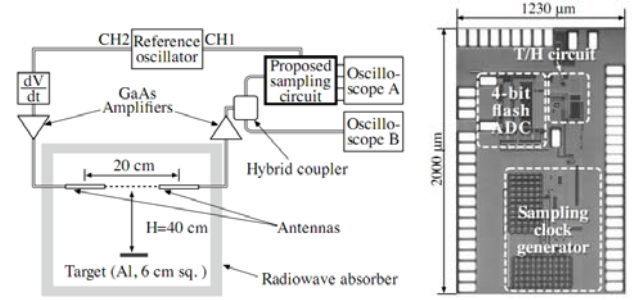


Fig. 4 Measurement setup.

Fig. 5 Die photograph.

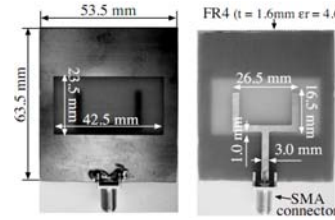


Fig. 6 UWB slot antenna.

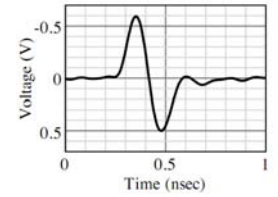


Fig. 7 Input GMP signal.

Table I Specification of the Proposed Sampling Circuit

Technology	65 nm CMOS process
Supply voltage	1.3V
PLL jitter	3.7 psec
Sampling rate	28.6 GS/s
Power consumption	50.7 mW
Die size	1.23 mm x 2.00 mm

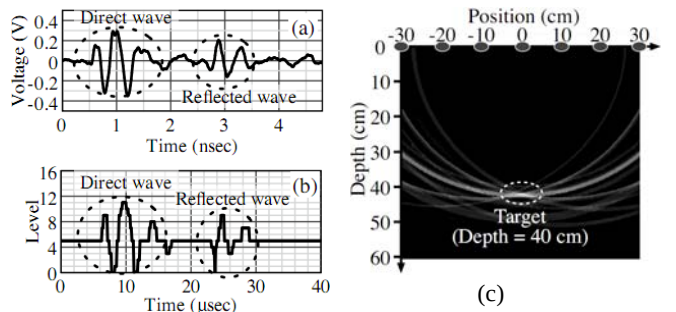


Fig. 8 (a) Input waveform of sampling circuit. (b) Output waveform of sampling circuit. (c) Confocal image from digital received waveforms.