

Wide-Frequency-Range Low-Noise Injection-locked Ring VCO for UWB Applications in 90 nm CMOS

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1. Introduction

Recently, one-chip RF LSI system solutions that can support multiple wireless services have been desired for lowering cost. To meet this, multiband and wideband scalable RF CMOS circuit technologies that can handle services from a wide frequency range have been required. However, it is very difficult to scale down RF/analog circuit blocks because of the presence of passive devices that do not follow the scaling trends of MOS transistors.

Ring oscillator-based voltage-controlled oscillators (ring VCOs) are attractive in terms of the area and the frequency tuning range. But, unfortunately, they have poor phase-noise characteristics, and therefore ring VCOs cannot be used for such real-world applications as cellular phones and wireless LANs. This paper concerns a method which is to try to lower the phase noise of a ring VCO with an injection locking technique for UWB applications [1].

2. Design of the Wide-Frequency-Range Injection-Locked ring VCO

Fig. 1 shows a topology of a proposed delay cell. The delay cell of this ring VCO contains an nMOS latch that generates a delay by positive feedback in order to satisfy the oscillation condition [2]. In addition, by eliminating the tail current source, the low frequency flicker noise is reduced because flicker noise is mainly contributed by the tail current source [3]. Such one is usually called a pseudo-differential delay cell. Also, it occupies small area because only 18-MOSFETs are used which consist the ring VCO. Moreover, it can generate I/Q signals which are necessary in RF-front end, too.

The oscillation frequency is decided by the ratio between the inverter size of a ring and a latch, and controlled by changing the inverter size of ring as to of a latch. The pMOS resistive loads are used for tuning the output oscillation frequency. In the commonly used delay cells with pMOS resistive loads, the range of control voltages. In the proposed delay cell, the pMOS transistors into which the bias-level-shifted control bias, biasn are inputted are added in order to make the range of sensitive voltages identical to the rail-to-rail voltage range (Fig. 2). Also the total equivalent resistance of the two pMOS transistors in parallel changes fairly linearly with the main control voltage, bias. Thus, the oscillation frequency can be tuned linearly. Fig. 2 also shows the schematic of the bias-level-shift circuit. The bias level shifted by 0.6V, biasn is generated by this circuit.

The VCO is based on a two-stage differential ring oscillator for oscillation in the ultra-wide-band of 3.1-10.6

GHz. To achieve subharmonic injection locking, nMOS switches are connected at the differential output node of each delay cell. The rail to rail pulses are injected into one of them for the injection locking, which are generated by an external signal generator.

3. Measurement Results

Fig. 3 shows a chip micrograph of the proposed VCO. It was fabricated by a 90 nm CMOS process. The proposed VCO occupies an area of $0.018 \text{ mm} \times 0.030 \text{ mm}$ including a bias-level-shift circuit. It was measured in 1.0V supply condition. Frequency tuning range was measured using an Agilent Technologies E4448A spectrum analyzer, which was shown 2.62-10.5 GHz in Fig. 4. Fig. 5 shows that the spurious levels at $f_0=10 \text{ GHz}$ with injection locking ($f_{inj}=500 \text{ MHz}$, pulse width: 71.4 ps) was -25.7 dBc. Injection signals were generated by an Anritsu MP1800A pulse pattern generator. The phase noise in that condition was measured by an Agilent Technologies E5052B signal source analyzer. A 1-MHz-offset phase noise of -72.8 dBc/Hz was generated in the VCO when the VCO in free-running condition. With injection locking ($f_{inj}=500 \text{ MHz}$, pulse width: 71.4 ps), a 1-MHz-offset phase noise of -119 dBc/Hz was generated. The total power consumption of the core circuit at $f_0=10 \text{ GHz}$ was 10.4 mW.

4. Conclusions

We proposed a scalable, wide-frequency-range and low-noise injection-locked VCO. It only occupied a small area of $0.018 \text{ mm} \times 0.030 \text{ mm}$. By using a bias-level-shift circuit and pMOS resistive loads, we obtained wide frequency tuning range of 2.62-10.5 GHz. Also by using an injection locking technique, we achieved a 1-MHz-offset phase noise of -119 dBc/Hz at $f_0=10 \text{ GHz}$ with comparable power consumption.

Acknowledgements

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References

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- [2] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2001.
- [3] J. Choi, K. Lim and J. Laskar, *IEEE Radio Frequency Integrated Circuits Symposium* (2008) 395.

Table I Performance Summary

	This Work
CMOS process [nm]	90
Power Supply [V]	1.0
Frequency Tuning Range [GHz]	2.62-10.5
Power Consumption at 10 GHz [mW]	10.4
Phase noise at 10 GHz (free-running) [dBc/Hz@1 MHz]	-72.8
Phase noise at 10 GHz (with inj.) [dBc/Hz@1 MHz]	-119
Area [mm ²]	0.018×0.030

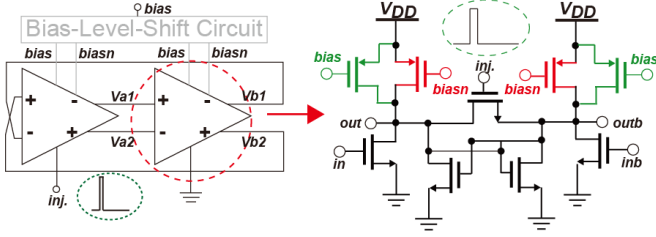


Fig. 1 Proposed differential ring VCO.

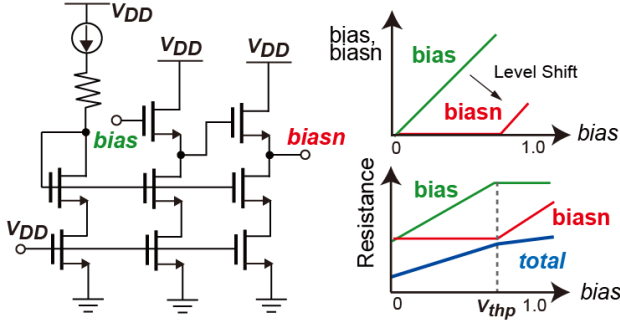


Fig. 2 Topology of a bias-level-shift circuit.

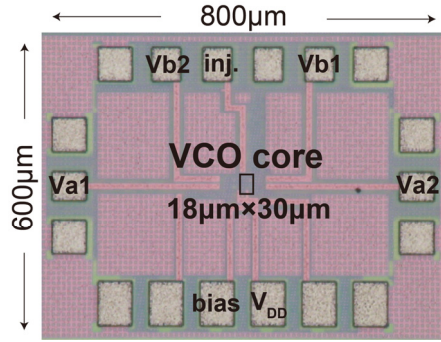


Fig. 3 A micrograph of the proposed ring VCO.

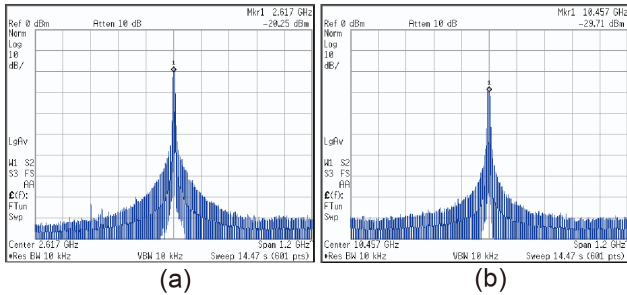


Fig. 4 Measured frequency spectra (2.62-10.5 GHz) by a spectrum analyzer when (a) bias=1 V, and (b) bias=0 V.

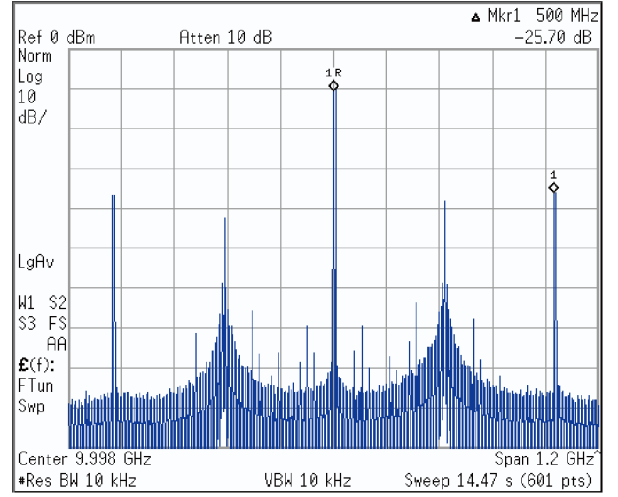


Fig. 5 Measured output frequency spectrum at $f_0 = 10$ GHz with $f_{inj} = 500$ MHz (pulse width: 71.4 ps).

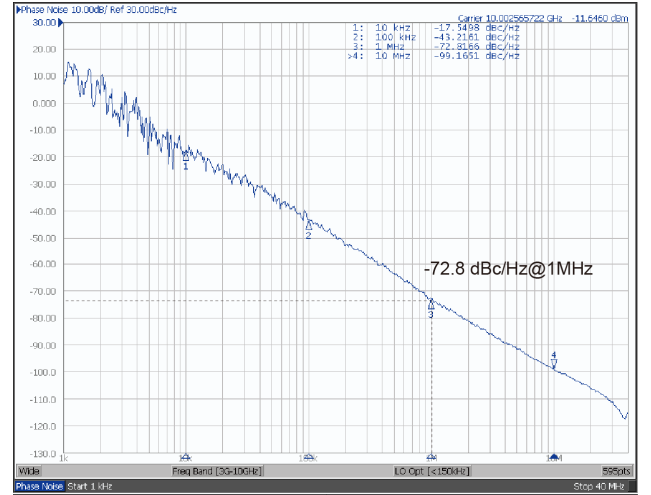


Fig. 6 Measured phase noise characteristic at $f_0 = 10$ GHz w/o injection locking.

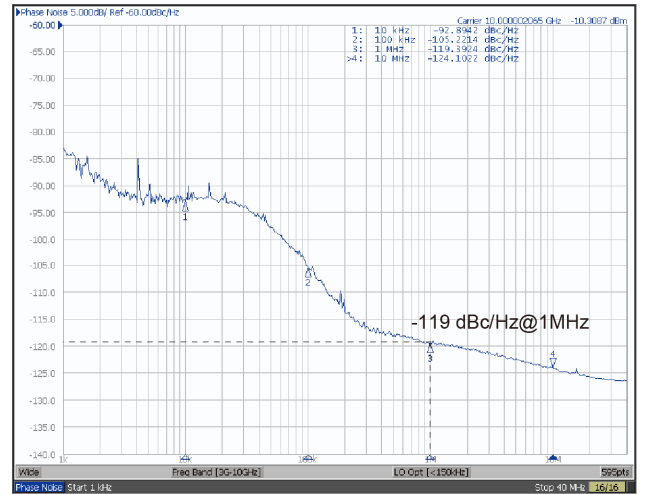


Fig. 7 Measured phase noise characteristic at $f_0 = 10$ GHz with $f_{inj} = 500$ MHz (pulse width: 71.4 ps).