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# A Practical Modeling Solution for Nanodevices with Strain Engineering

David Chen, Ryan Lee, U C Liu, Michael Yeh, Burnie Huang, M F Wang, G S Lin, M K Tsai, J H Lai, and C S Yeh

Modeling Division, Advanced Technology Development, United Microelectronics Corporation, Hsinchu, Taiwan.

Phone: +886-3-5782258, Fax: +886-3-5785076, e-mail: c_s_yeh@umc.com

**Abstract**

A compact model solution for modeling layout-dependent effects in CMOS nanotechnology with strain engineering is proposed. Strain engineering enhances device performance but causes significant layout-dependent effects, including poly spacing effect (PSE), boundary effect (BE), and neighboring diffusion effect (NDE). If these effects are not well modeled, pre-layout and post-layout simulations will have significant differences. Silicon verification based upon 40nm technology is demonstrated.

## 1. Introduction

Strain engineering, including dual stress liners (DSLs) and SiGe, is widely used to enhance carrier mobility in 40nm and beyond technologies applied in high-speed logic and mixed-signal chip design [1][2]. In DSL, a tensile contact etching stop layer (T-CESL) is used to enhance nMOS mobility and a compressive CESL (C-CESL) is used for pMOS mobility. SiGe is used to further enhance pMOS mobility. Combination of strain engineering and aggressive device scaling results in significant layout-dependent effects. Without proper modeling of these layout-dependent effects, differences between silicon data and model simulation can exceed 12%.

In this work, modeling equations for layout-dependent effects including PSE, BE and NDE with scalability in geometry and bias are proposed. Subcircuits are modeled for these equations in BSIM4 and verified in 40nm technology.

## 2. Modeling for Layout-Dependent Effects

TEM pictures and a brief description of the process flow used to fabricate the devices for device characterization and model development are shown in Fig. 1. DSLs are used for both nMOS and pMOS as CESL layers after the formation of gate poly, halo, source/drain, spacers and salicidation. Nominal gate length is 36nm in the drawn layer and 32nm in TEM for both nMOS and pMOS. SiGe is formed in the source/drain regions of pMOS. Development of modeling equations for PSE, BE, and NDE is focused on the improvement of existing equations for threshold voltage and mobility in BSIM4.

**(A) PSE**: This effect is mainly caused by the CESL for both nMOS and pMOS on the gate poly. Poly finger number and poly spacing affect device performance. Based upon the characterization, the first and the second poly have significant impact on device performance [3][4]. Fig. 2 shows the typical layout to define the instance parameters for the first poly. SGA1, SGA2, SGB1, SGB2, WGA1, WGA2, WGB1, and WGB2 are extracted from the GDSII database by LVS (layout versus schematic) to calculate the instance parameters SGA and SGB. The newly added modeling parameters for threshold voltage are SGAREF, SGBREF, XLSG, XWSG, KPVTH0, LODKPETA0, KPETA0, LKPETA0, WKPETA0, PKPETA0, LKPVTH0, WKPVTH0, LLODKPVTH, WLODKPVTH and PKPVTH0. For mobility, the newly added model parameters are KPU0, LKPU0, WKPU0, LLODKPU0, WLODKPU0, PKPU0, and TKPU0. Model equations and the new model parameters for the first poly are shown in Fig. 2. Based upon the device behavior check, the impact of the second poly on device performance is still significant and PSE model equations for the second poly are necessary. Fig. 3 shows the typical layout to define the instance parameters for the second poly. SG2A1, SG2A2, SG2B1, SG2B2, WG2A1, WG2A2, WG2B1, and WG2B2 are extracted from a GDSII database by LVS to calculate instance parameters SG2A and SG2B. PSE model equations for the second poly are similar to those of the first poly. The only difference is that the number “2” is added to every new model parameter of the first poly to become the new model parameters of the second poly.

**(B) BE**: This effect is also caused by CESL. The boundary of the tensile and compressive layers is defined by a well. Tensile (compressive) layers will have some impact on the nMOS (pMOS) close to the N-well (P-well). Fig. 4 shows the typical layout to define the instance parameters for BE. NBXA, NBXB, FNXA, FBXB, NBYA, NBYB, FBYA and FBYB are the instance parameters for both x and y directions and are extracted by LVS. Threshold voltage and mobility model equations for the x direction are shown in Fig. 4. NBXAREF, NBXBREF, KDXVTH0, LKDXVTH0, WKDXVTH0, PKDXVTH0, LLODKDXVTH, WLODKDXVTH, KDXETA0, LKDXETA0, WKDXETA0, PKDXETA0, and LODKDXETA0 are new model parameters for threshold voltage. KDXU0, LKDXU0, WKDXU0, PKDXU0, LLODKDXU0, WLODKDXU0, TKDXU0, and KDXVSAT are new parameters for mobility. Model equations for the y direction are similar to those of the x direction; the only difference is that “X” is changed to “Y.”

**(C) NDE**: Fig. 5 shows the typical layout to define the instance parameters for NDE. Instance parameters NDEXA1, NDEXA2, NDEXB1, and NDEX2 are for the x direction; NDEYA1, NDEYA2, NDEYB1 and NDEYB2 are for the y direction. Model equations for the x direction on the right side are shown in Fig. 5. New model parameters of threshold voltage are NDEXAREF, NDEXAVTH0, LNDEXAVTH0, WNDEXAVTH0, PNDEXAVTH0, LLODNDEXAVTH0, WLODNDEXAVTH0, NEDXAETA0, LNDEXAETA0, WNDEXAETA0, and PNDEXAETA0. New mobility parameters are NDEXAU0, LNDEXAU0, WNDEXAU0, PNDEXAU0, LLODNDEXAU0, WLODNDEXAU0, TNDEXAU0, NDEXAVSAT, LNDEXAVSAT, WNDEXAVSAT, and PNDESAVSAT. For the y direction, model equations are similar to those in the x direction. The only difference is that “X” is replaced with “Y.” Modeling of NDE needs to take into consideration the type of the neighboring diffusion. Fig. 6 defines the different modes for different combinations in both x and y directions.

## 3. Results and Discussion

Evaluation of model equations is focused on the variation of saturation current Ids. Fig. 7 shows Ids degradation versus SGA for the first poly in silicon and the PSE model. Ids has 12% (5%) degradation for nMOS (pMOS) when SGA increases from 0.126um to 0.288um. Impact of the second poly on Ids and model verification is shown in Fig. 8. Ids has about 4.2% (4.2%) degradation for nMOS (pMOS) when SG2A increases from 0.306um to 0.45um. Model simulation results based upon the proposed PSE model equations for both the first and the second poly have excellent agreement with the measurement data. Fig. 9 shows Ids variation versus spacing NBXA in the x direction. Ids has 6.5% (8.5%) degradation for nMOS (pMOS) when NBXA increases from 0.171um to 1.8um. Fig. 10 shows Ids variation versus NBYA. Ids has 0.8% (-3%) variation for nMOS (pMOS) when NBYA increases from 0.072um to 1.8um. Fig. 9 and Fig. 10 demonstrate that BE modeling has excellent accuracy. Fig. 11 shows Ids variation versus NDEX. Ids has 1.8% (1.8%) degradation for nMOS (pMOS) with NDEXMOD = 1 (NDEXMOD = 3) when NDEX increases from 0.072um to 1.8um. Fig. 12 shows Ids variation versus NDEY. Ids has 2.5% (1.8%) degradation for nMOS (pMOS) with NDEYMOD = 3 (NDEYMOD = 1) when NDEY increases from 0.144um to 1.8um. Fig. 11 and Fig. 12 show that measurement data and the NDE model match well. Table 1 shows the model verification for ring oscillators INVERTER (inv, inv3), NAND (nd, nd3), and NOR (nr, nr3) with F.O. = 1 and 3. All effects, viz. LOD, WPE, PSE, BE, and NDE, are included. PSE, BE, and NDE have an 8% – 12% impact on circuit performance.

### 4. Summary

Model equations for layout-dependent effects including PSE, BE, and NDE caused by strain engineering are proposed and successfully verified. These model equations are set up as subcircuits in BSIM4. These significant effects should be included in the pre-simulation stage to optimize design efforts.

## References

[1]. P. R. Chidambaram, et. al., *IEEE T-ED*, vol. 53, pp. 944-964, 2008.
[2]. S. S. Chung, et. al., *IEDM Tech. Dig.*, pp. 1-4, Dec. 2008.
[3]. L. Ge, et. al., *Proc. SOI Conf.*, pp. 25-26, Oct. 2007.
[4]. H. Tsuno, et. al., *Symp. VLSI Tech.*, pp. 204-205, June 2007.

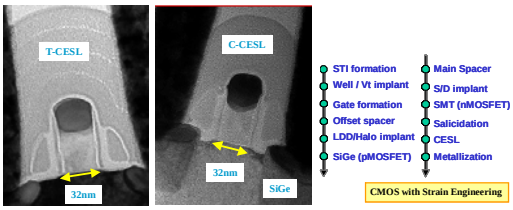
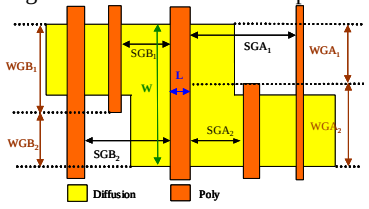



Fig.1. A TEM result and brief process flow.




$$VTH0 = VTH0_{original} + \frac{KPVTH0}{KPstress\_vth0}\cdot(Inv\_sga + Inv\_sgb - Inv\_sga_{ref} - Inv\_sgb_{ref})$$

$$ETA0 = ETA0_{original} + \frac{KPETA}{KPstress\_vth0^{LODKPETA0}}\cdot(Inv\_sga + Inv\_sgb - Inv\_sga_{ref} - Inv\_sgb_{ref})$$

$$KPETA = KPETA0 + \frac{LKPETA0}{(L+XLSG)} + \frac{WKPETA0}{(W+XWSG)} + \frac{PKPETA0}{(L+XLSG)\cdot(W+XWSG)}$$

Where

$$Inv\_sga_{ref} = \frac{1}{SGAREF + XLSG + 0.5\cdot L_{drawn}} \qquad Inv\_sgb_{ref} = \frac{1}{SGBREF + XLSG + 0.5\cdot L_{drawn}}$$

$$Inv\_sga = \frac{1}{SGA + XLSG + 0.5\cdot L_{drawn}} \qquad Inv\_sgb = \frac{1}{SGB + XLSG + 0.5\cdot L_{drawn}}$$

$$KPstress\_vth0 = 1 + \frac{LKPVTH0}{(L+XLSG)^{LLODKPVTH}} + \frac{WKPVTH0}{(W+XWSG)^{WLODKPVTH}} + \frac{PKPVTH0}{(L+XLSG)^{LLODKPVTH}\cdot(W+XWSG)^{WLODKPVTH}}$$

$$\rho_{diff}(SGA,SGB) = \frac{KPU0}{KPstress\_\mu0}\cdot(Inv\_sga + Inv\_sgb)$$

Where

$$KPstress\_\mu0 = \left(1 + \frac{LKPU0}{(L_{drawn}+XLSG)^{LLODKPU0}} + \frac{WKPU0}{(W_{drawn}+XWSG)^{WLODKPU0}} + \frac{PKPU0}{(L_{drawn}+XLSG)^{LLODKPU0}\cdot(W_{drawn}+XWSG)^{WLODKPU0}}\right)\times\left(1 + TKPU0\cdot\left(\frac{Temperature}{TNOM} - 1\right)\right)$$

Fig.2. A typical layout to define instance parameters [3] and model equations of the first poly in PSE.

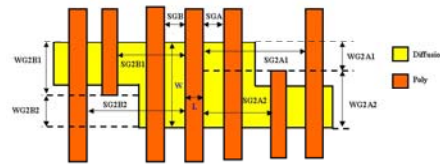
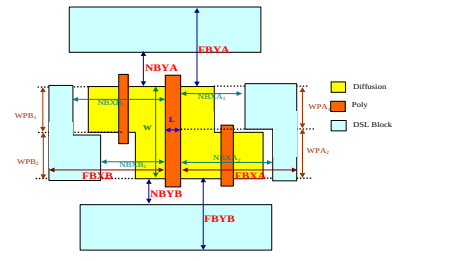



Fig.3. A typical layout to define instance parameters of the second poly in PSE.




$$VTH0 = VTH0_{original} + \frac{KDXVTH0}{KDXstress\_vth0}\cdot(Inv\_nbxa + Inv\_nbxb - Inv\_nbxa_{ref} - Inv\_nbxb_{ref})$$

$$ETA0 = ETA0_{original} + \frac{KDXETA}{KDXstress\_vth0^{LODKDXETA0}}\cdot(Inv\_nbxa + Inv\_nbxb - Inv\_nbxa_{ref} - Inv\_nbxb_{ref})$$

$$KDXETA = KDXETA0 + \frac{LKDXETA0}{(L+XL)} + \frac{WKDXETA0}{(W+XW)} + \frac{PKDXETA0}{(L+XL)\cdot(W+XW)}$$

Where

$$Inv\_nbxa_{ref} = \frac{1}{NBXAREF + XL + 0.5\cdot L_{drawn}} \qquad Inv\_nbxb_{ref} = \frac{1}{NBXBREF + XL + 0.5\cdot L_{drawn}}$$

$$Inv\_nbxa = \frac{1}{NBXA + XL + 0.5\cdot L_{drawn}} \qquad Inv\_nbxb = \frac{1}{NBXB + XL + 0.5\cdot L_{drawn}}$$

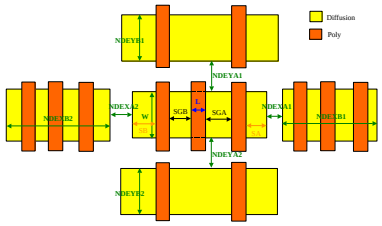
$$KDXstress\_vth0 = 1 + \frac{LKDXVTH0}{(L+XL)^{LLODKDXVTH}} + \frac{WKDXVTH0}{(W+XW)^{WLODKDXVTH}} + \frac{PKDXVTH0}{(L+XL)^{LLODKDXVTH}\cdot(W+XW)^{WLODKDXVTH}}$$

$$\rho_{diff}(NBXA,NBXB) = \frac{KDXU0}{KDXstress\_\mu0}\cdot(Inv\_nbxa + Inv\_nbxb)$$

Where

$$KDXstress\_\mu0 = \left(1 + \frac{LKDXU0}{(L_{drawn}+XL)^{LLODKDXU0}} + \frac{WKDXU0}{(W_{drawn}+XW)^{WLODKDXU0}} + \frac{PKDXU0}{(L_{drawn}+XL)^{LLODKDXU0}\cdot(W_{drawn}+XW)^{WLODKDXU0}}\right)\times\left(1 + TKDXU0\cdot\left(\frac{Temperature}{TNOM} - 1\right)\right)$$

Fig.4.A typical layout to define instance parameters and model equations of BE.




$$VTH0 = VTH0_{original} + \frac{NDEXAVTH0}{NDEXAstress\_vth0}\left(\frac{Inv\_ndexa_1 + Inv\_ndexa_2 - Inv\_ndexa_{1ref}}{-Inv\_ndexa_{2ref}}\right)$$

$$ETA0 = ETA0_{original} + \frac{NDEXAETA}{NDEXAstress\_vth0^{LODNDEXAETA0}}\left(\frac{Inv\_ndexa_1 + Inv\_ndexa_2 - Inv\_ndexa_{1ref}}{-Inv\_ndexa_{2ref}}\right)$$

$$NDEXAETA = NDEXAETA0 + \frac{LNDEXAETA0}{(L_{drawn}+XL)} + \frac{WNDEXAETA0}{(W_{drawn}+XW)} + \frac{PNDEXAETA0}{(L_{drawn}+XL)\cdot(W_{drawn}+XW)}$$

Where

$$Inv\_ndexa_{1ref} = \frac{1}{NDEXAREF + SAREF} \qquad Inv\_ndexa_{2ref} = \frac{1}{NDEXAREF + SBREF}$$

$$Inv\_ndexa_1 = \frac{1}{NDEXA1 + SA} \qquad Inv\_ndexa_2 = \frac{1}{NDEXA2 + SB}$$

$$NDEXA\ stress\_vth0 = 1 + \frac{LNDEXATH0}{(L_{drawn}+XL)^{LLODNDEXAVTH}} + \frac{WNDEXAVTH0}{(W_{drawn}+XW)^{WLODNDEXAVTH}} + \frac{PNDEXAVTH0}{(L_{drawn}+XL)^{LLODNDEXAVTH}\cdot(W_{drawn}+XW)^{WLODNDEXAVTH}}$$

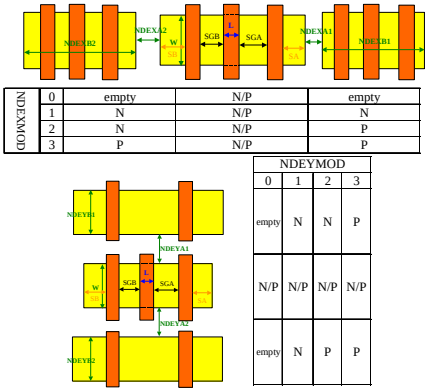
$$\rho_{diff}(NDEXA1,NDEXA2) = \frac{NDEXAU0}{NDEXAstress\_\mu0}\cdot(Inv\_ndexa_1 + Inv\_ndexa_2)$$

$$NDEXAVSAtotal = \left(NDEXAVSAT + \frac{LNDEXAVSAT}{(L_{drawn}+XL)} + \frac{WNDEXAVSAT}{(W_{drawn}+XW)} + \frac{PNDEXAVSAT}{(L_{drawn}+XL)\cdot(W_{drawn}+XW)}\right)$$

Where

$$NDEXAstress\_\mu0 = \left(1 + \frac{LNDEXAU0}{(L_{drawn}+XL)^{LLODNDEXAU0}} + \frac{WNDEXAU0}{(W_{drawn}+XW)^{WLODNDEXAU0}} + \frac{PNDEXAU0}{(L_{drawn}+XL)^{LLODNDEXAU0}\cdot(W_{drawn}+XW)^{WLODNDEXAU0}}\right)\times\left(1 + TNDEXAU0\cdot\left(\frac{Temperature}{TNOM} - 1\right)\right)$$

Fig.5. A typical layout to define instance parameters of NDE and model equations.




| NDEXAMOD | 0 | empty | N/P | empty |
|---|---|---|---|---|
| | 1 | N | N/P | N |
| | 2 | N | N/P | P |
| | 3 | P | N/P | P |

| NDEYMOD | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| empty | N | N | P | |
| N/P | N/P | N/P | N/P | |
| empty | N | P | P | |

Fig.6. Different mode combination and setup for NDE modeling.

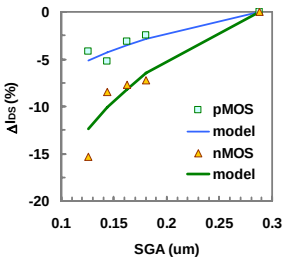



Fig.7. $I_{ds}$ variation vs. SGA (first poly) for PSE characterization and model verification.

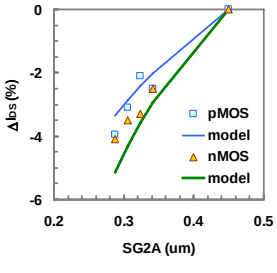



Fig.8. $I_{ds}$ variation vs. SG2A (2nd Poly) for PSE characterization and model verification.

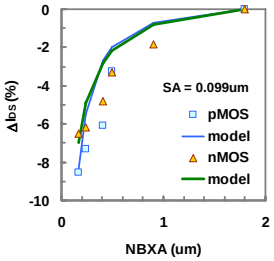



Fig.9. $I_{ds}$ variation vs. NBXA for BE characterization and model verification.

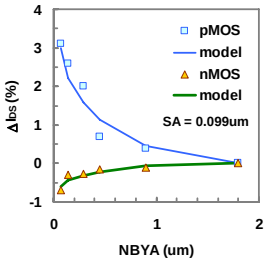



Fig.10. $I_{ds}$ variation vs. NBYA for BE characterization and model verification.

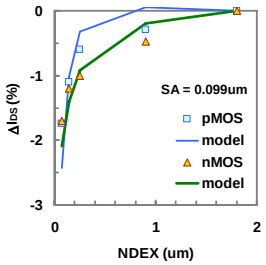



Fig.11. $I_{ds}$ variation vs. NDEX for NDE characterization and model verification.

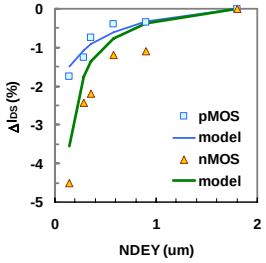



Fig.12. $I_{ds}$ variation vs. NDEY for NDE characterization and model verification.

Table 1. Impact analysis for LOD, WPE, PSE, BE and NDE for circuit level.

| unit: ps/stage | inv | inv3 | nd | nd3 | nr | nr3 |
|---|---|---|---|---|---|---|
| WPE + LOD | 3.89 | 5.72 | 8.16 | 11.92 | 9.97 | 11.92 |
| All Effects | 4.2 | 6.17 | 8.78 | 12.86 | 11.16 | 13.36 |
| Difference | 8% | 7.88% | 7.60% | 7.90% | 11.93% | 12.20% |

$W_n / W_p / L$ = 0.3um / 0.5um / 0.036um