Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp802-803

Analysis of Within-Die and Die-to-Die CMOS-Process Variation With Reconfigurable Ring-Oscillator Arrays

T. Ansari, W. Imafuku, A. Kawabata, M. Yasuda, T. Koide, and H. J. Mattausch

Research Institute for Nanodevice and Bio Systems, Grad. School of Advanced Sciences of Matter, Hiroshima University.
739-8527, Higashi-Hiroshima, Kagamiyama 1-4-2, Japan. Phone: +81-082-424-6265 E-mail: ansaritania@hiroshima-u.ac.jp

1. Introduction

Process related variations are major concerns in advanced CMOS technologies [1-3]. Here, we analyzed the stage-delay variation in ring oscillator arrays, fabricated in 180nm CMOS technology, with large stage numbers and flexible replacement possibility for all ring oscillator stages. This allows an experimental analysis of the 2-dimensional properties of the within-die (WID) variation over the 1.69 mm × 1.59 mm area covered by the ring oscillators. Our results show that the variation over this large area is still mainly of Gaussian nature. Simulation with the HiSIM model [4], using independently determined data for HiSIM-model-parameter WID-variation [2, 3], is suitable to predict the measured WID variation of the delay stages in these ring oscillator arrays.

2. Test circuit and measurement setup

The test chip consists of ring oscillators arranged in rows on a 2.5 mm×2.5 mm chip designed and fabricated in 180 nm CMOS technology [Fig.1]. Each ring oscillator has 256 adjustable delay stages and a NAND gate for ring oscillator activation [Fig.2]. All delay stages are designed identical with a selectable delayed or non-delayed signal path. The layout has a length of 1690 μm , a width of 15 μm and stacks the delay stages into 128 upper stages and 128 lower stages to minimize signal routing length between the stages. The ring oscillators are separated by 24 μm from one another to allow space for storing the path-select circuitry of stages for each ring oscillator.

In the measurement setup, the delay-selection signals are processed from a logic analyzer and the frequencies are captured with the help of a frequency meter.

3. Measurement results and correlation with simulation

3.1 Variation measurements along horizontal direction:

To determine the variation in horizontal direction, the frequencies where all stages are set to the non-delayed path and where only one stage is set to the delayed path, are measured. The stage with the delayed path is changed to different positions in the ring oscillator. Table I shows the measured mean stage-delay times (μ) for 8 ring oscillators at different vertical positions in the die and for 3 different dies. The corresponding sigma values (σ) for the variation of the stage delays in horizontal direction of each ring oscillator are also listed. The data for each die has a slight trend for the mean stage delay (μ), which is somewhat larger for the ring oscillators located in the upper section of the die. This may point to a parametric component of the WID variation in vertical direction, but may also be explained by a small drift which we noticed in the measurement set-up. The σ values for the delay-stage variation in horizontal direction change randomly and have no correlation with one another. This lack of correlations confirms the absence of any parametric horizontal WID-variation effects over a distance of 1690 μm . Also, the voltage dependence of the ring-oscillator-frequency changes due to a single delayed stage is 170 KHz at VDD=1.8 V and 27.3 KHz at VDD=0.9 V (Fig.3). A clear separation from the frequency where none of the stages is in delayed condition is verified. However, the horizontal variation can be seen to increase by about a factor 2.5, when Vdd is lowered from 1.8 V to 0.9 V. Histograms, Gaussian fits and corresponding mean and sigma values for the combined delayed-stage variations from all 8 ring oscillators, which are a measure of the complete WID variation over the 1690 μm ×1590 μm area, are shown for the 3 dies in Fig.4, Fig.5 and Fig.6. There is some data separated from the main distribution for die 2 and 3, which may result from a drift in the absolute accuracy of the measurement set up.

3.2 Variation measurements in vertical direction:

Fixed positions of the delayed stage in horizontal direction at different vertical positions have also been measured to analyze the vertical variation. Table II shows the mean stage-delay values μ and the corresponding σ for the vertical variation of the delayed signal path in 5 different dies. The μ values are almost the same as that in horizontal direction. However, the σ values for the variation are clearly larger than in horizontal direction which again suggests that there may be some systematic variations present in the vertical direction of the dies.

The Monte Carlo simulation is done with the data for WID parameter variation of the HiSIM Model [2, 3] shown in Table III. The result of this simulation for WID variation of the delayed stage path is shown in Fig.7. The mean value of the simulated path delay is up to a factor 1.2 shorter than for the measured path delays. This may be attributed to the fact that the HiSIM parameters were determined from a different production lot. The simulated σ value for the variation falls within the range of the 3 measured dies, which suggests that the WID variation can be assumed to be random and approximately the same for different dies from the same wafer and maybe even from different wafers and lots.

4. Conclusions

Here, we reported the measured two-dimensional WID variation of a time-delay stage, consisting of 4 inverters and a capacitor, over an area of 1690 μm ×1590 μm . The time-delay stage is embedded in large ring oscillators and can be switched to different positions of the ring oscillators,

which are arranged in a 2-dimensional array. It is found that the variation is small in comparison to the stage delay and does not change from die to die for the same wafer. The break-down into horizontal and vertical component suggests that a parametric variation in vertical direction may be present for the analyzed wafer.

Acknowledgements

The VLSI chip in this study has been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with STARC, Rohm Co., Cadence Design Systems Inc. and Simucad Design Automation Inc.

References

[1] K. J. Kuhn,.;Proc. IEDM (2007), pp. 471-474
[2] K. Joguchi el; SSDM(2009), D-7-3.
[3] A.Kaya el; SASIMI(2009), pp. 446-449
[4] M. Miura-Mattausch et al., IEEE TED 53, pp. 1994-2007 (2006)

Table I. Test data for horizontal variation of a single delayed stage

Row position	Sigma (σ) ns	Mean (μ) ns	Sigma (σ) ns	Mean (μ) ns	Sigma (σ) ns	Mean (μ) ns
	Die 1		Die 2		Die 3	
1	0.0021	0.955	0.0064	0.954	0.0054	0.996
2	0.0027	0.924	0.0033	0.841	0.0053	0.865
3	0.0031	0.925	0.0047	0.832	0.0035	0.862
4	0.0071	0.895	0.0039	0.839	0.0023	0.825
5	0.0038	0.906	0.0055	0.841	0.0038	0.853
6	0.0028	0.888	0.0071	0.807	0.0029	0.842
7	0.0027	0.871	0.0046	0.830	0.0055	0.841
8	0.0088	0.836	0.0067	0.859	0.0038	0.818

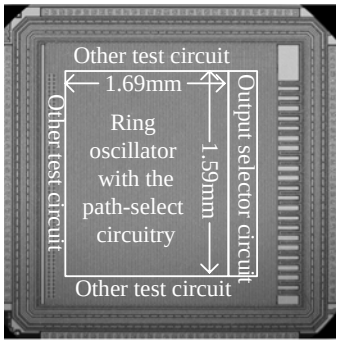


Fig.1 Micrograph of the fabricated test chip

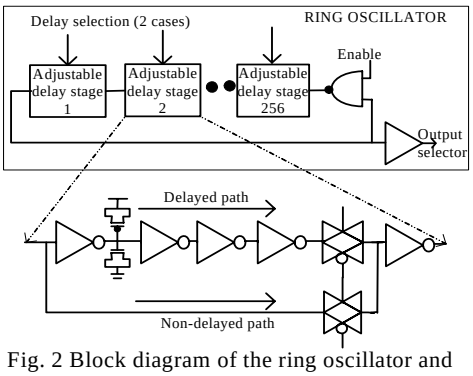


Fig. 2 Block diagram of the ring oscillator and basic structure of a 'single stage'

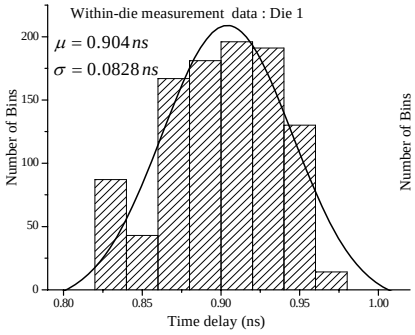


Fig.4 : Histogram and Gaussian curve of the stage delay within the first die

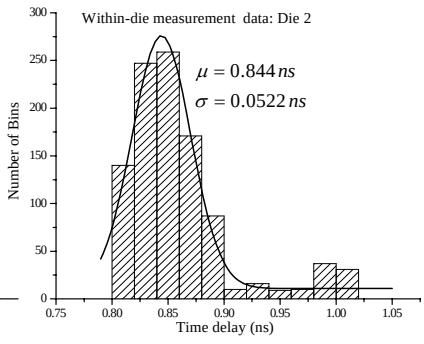


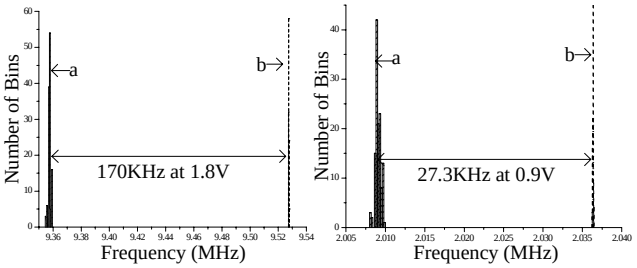
Fig.5 : Histogram and Gaussian curve of the stage delay within the second die

Table II. Test data of the vertical variation analysis for a single delayed stage

	Mean (μ)ns	Sigma (σ)ns
Die 1	0.847	0.0133
Die 2	0.822	0.0154
Die 3	0.862	0.0081
Die 4	0.826	0.0488
Die 5	0.845	0.0336

Table III. Data of the HiSIM WID-parameter variation used for the simulation

HiSIM Para-meter	PMOS	NMOS
NSUBC [%]	± 0.8	± 1.2
NSUBP [%]	± 0.9	± 1.0
XLD [nm]	± 1.0	± 2.5



a=Variation with a single stage in delayed path at different position in a ring oscillator and all other stages in non-delayed path.
b=Repeated measurements(~60 times) for the same ring oscillator with all stages in non-delayed path to verify measurement accuracy.

Fig. 3: Measured frequency difference due to a delay stage at nominal (1.8V) and reduced (0.9V) supply voltage for a ring oscillator and its variation for different stage locations.

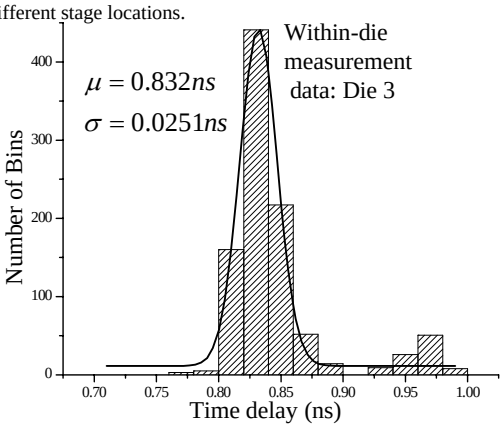


Fig.6 : Histogram and Gaussian curve of the stage delay within the third die

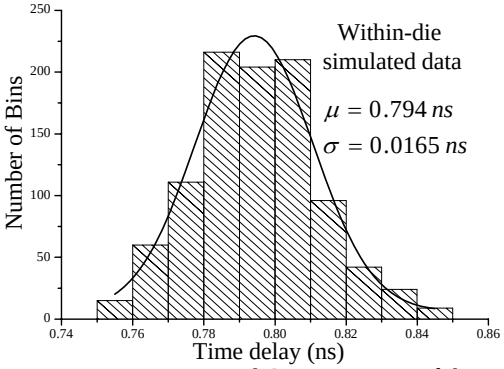


Fig.7 : Histogram and Gaussian curve of the stage delay by Monte Carlo simulation using the HiSIM model and independently determined WID variation from a different lot[2,3].