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Large Scale Test Circuits for Systematic Evaluation of Variability and Noise of MOSFETs' Electrical Characteristics

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1. Introduction

Variation of the electrical characteristics of MOSFETs such as drain-source current (I_{ds}), subthreshold swing factor (S-factor), threshold voltage (V_{th}), junction leakage current (I_{jleak}), and gate leakage current (I_{Gleak}) as well as their random noise have been critical issues for the reduction of power consumption for various applications of LSI[1-2]. In order to accurately evaluate these variation and noise, statistical measurements of a large number of MOSFETs comparable to the actual products are indispensable. We have investigated the measuring methods for these issues [3-6]. By combining these test circuits, a systematic evaluation of various statistic parameters of characteristics becomes available. Since the developed test circuits is so simple, we can evaluate the impacts of the various manufacturing processes and device parameters to the variation and noise characteristics. In this paper, we report the evaluating key concept and technology including the test circuit structure with the important results of these circuits.

2. Test circuit

For statistical evaluation, the electrical properties for each MOSFET have to be measured in a very short period. Then, a large number of unit cells including devise under test (DUT) are set in a large array. In the unit cells, voltage signal that corresponds to the target current is readout using source follower amplifier. Fig. 1(a) shows concept of the circuit measuring I_{ds}. The measured MOSFET and current source construct source follower circuit through a select switch. V_{gs} corresponding I_{ds} is expressed as $V_{gs} = V_G - V_{OUT}$. I_{ds}-V_{gs} characteristic are measured by changing the I_{REF} controlling the current source. S-factor is extracted from the I_{ds}-V_{gs} characteristic, represented as $S=d(\log I_{ds})/dV_{gs}$. I_{ds} RTS noise of measured MOSFET appears as V_{gs} fluctuation in time scale corresponding to the I_{ds}. Fig. 1(b) shows concept of the circuit for measuring I_{jleak}. DUT's source terminal connected to gate of source follower transistor. I_{jleak} is converted to a voltage signal at the capacitor in the unit cell. When DUT turns on , V_{jleak} is reset to V_{reset}. After turning off DUT, change in V_{jleak} is sampled continuously. I_{jleak} is represented as $I_{jleak} = C_{jleak}dV_{jleak}/dt$. Fig. 1(c) shows concept of circuit mearureing I_{Gleak}. DUT's source/drain terminals connect to source follower transistor through common gate transistor and readout switch (RD). I_{Gleak} is converted to a voltage signal V_{Gleak} at the capacitor C_{Gleak}. Thanks to the common gate transistor, voltage of DUT's source/drain terminal is constant while V_{Gleak} is changed. Therefore, electric field across the gate oxide is constant. To apply a high voltage stress to the gate oxide of DUT for measuring stress induced leakage current, RD is turned off and the stress switch (ST) is turned on and high voltage is applied to V_{G_G}. To measure I_{Gleak}, ST is turned off and RD is turned on, and reset switch (R) is turn on to reset C_{Gleak}. After turning off R, a change in V_{Gleak} is sampled continuously. Fig. 2 shows array test circuit diagram. This is constructed with arrayed unit cell described in Fig. 1, a vertical shift resistor and a horizontal shift resistor for selecting the unit cell, current source transistor located on every column, the analog memories for temporary storing voltage signal at each column, and the output buffer for the amplification of the voltage signal and output the signal outside the chip. The shift resistors fast select the unit cells sequentially and voltage signal from unit cells are readout with source follower circuit, therefore measuring a large number of cells in a short period becomes possible. In this experiment, the measurement of the V_{th} of one million MOSFETs can be finished in 0.7s, I_{jleak} of more than 28000 samples in 7.7s with ten times averaging, I_{Gleak} of more than 87000 samples in 20s for one bias. In addition the test circuits are simple, these can operate in a various MOSFETs, which have different gate length, gate width, gate insulator films, thickness, doping concentration and profile, and so on. The test pattern is manufactured by a 0.35-μm 1-poly 1-metal CMOS technology and 0.22-μm 1-poly 2-metal CMOS technology.

3. Results

Fig. 3 shows measurement results of I_{ds}-V_{gs} characteristic of 65536 MOSFETs. Fig. 4 shows distribution of V_{th} for three MOSFET's sizes. The V_{th} variation increases with a decrease of the gate width. Fig. 5 shows distribution of S-factor extracted from of I_{ds}-V_{gs} characteristic as a function of antenna ratio that is a ratio of first metal layer area to gate area. The variation increases with increase in antenna ratio. Fig. 6 shows distribution of RTS of I_{ds} as a function of channel doping concentration (N_A). Noise intensity and occurrence frequency increase as N_A becomes higher. Fig. 7 shows distribution of I_{Gleak} for with and without stress. As stress time increase, tail cells increase. In very few cells of the tail cells, RTS of I_{Gleak} appears as shown in Fig. 8. In addition, RTS appears in I_{jleak}. Fig. 9 shows the distribution of σI_{jleak} in the time scale, that indicates noise intensity. σI_{jleak} increases with increase in temperature.

4. Conclusions

This test circuits can measure statistical characteristics of MOSFETs in short time and can operate when the gate size, doping concentration and other device parameters of measuring MOSFET are changed. In addition, RTS noise are detected in I_{ds}, I_{jleak} and I_{Gleak} by a fast sampling of the signals in the time scale. This developed test circuits is very efficient for systematic evaluation and useful to suppress the variability of electrical properties in MOSFETs.

References

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[6] K. Abe et al., Proc. IRPS, p. 683, 2010.

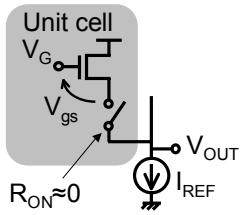
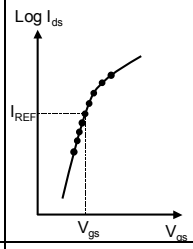
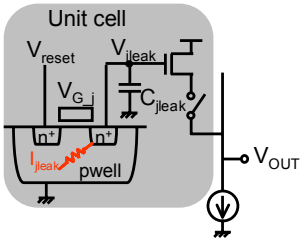
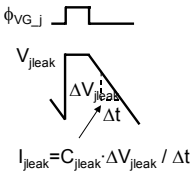
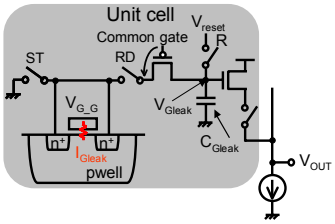
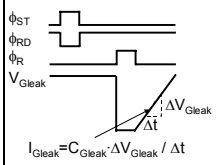
Measurement target	Equivalent circuit	Measurement method
(a)Drain-Source current (I_{ds}) ● V_{TH} ● S-factor ● RTS of I_{ds}		
(b)Source-Well current (I_{jleak}) ● Junction leakage ● RTS of I_{jleak}		
(c)Gate current (I_{Gleak}) ● Gate leakage with & w/o stress ● RTS of I_{Gleak}		

Fig. 1 Concept of three circuits measuring I_{ds}, I_{jleak} and I_{Gleak}.

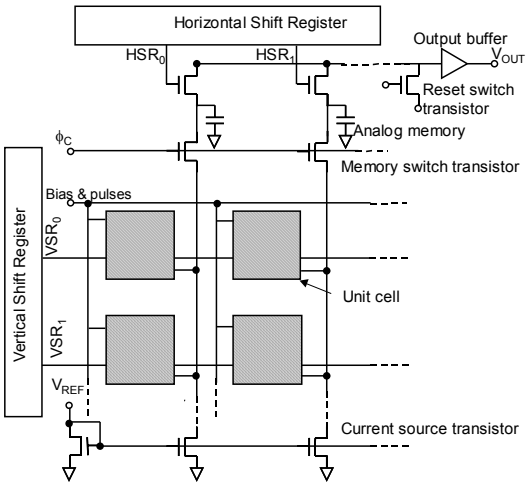


Fig. 2 Array circuit diagram for test pattern. The circuits in Fig. 1 are set in unit cell of this figure.

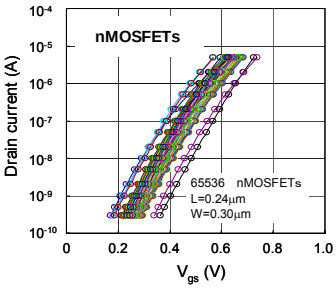


Fig. 3 Measurement results of Ids-Vgs characteristics for 65536 nMOSFETs.

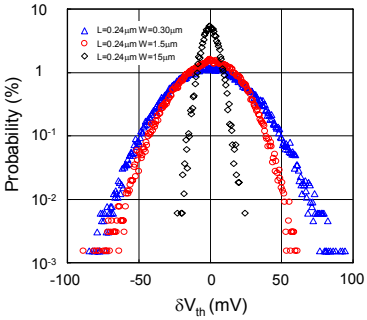


Fig. 4 Distribution of V_{th} for three MOSFET's sizes.

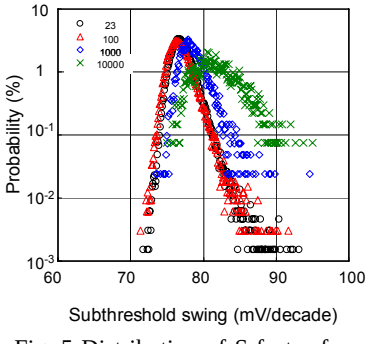


Fig. 5 Distribution of S-factor for nMOSFETs having antenna ratios of 23, 100, 1000 and 10000.

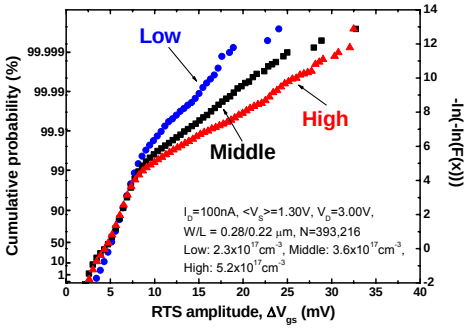


Fig. 6 Distribution of RTS amplitude for different channel doping concentration.

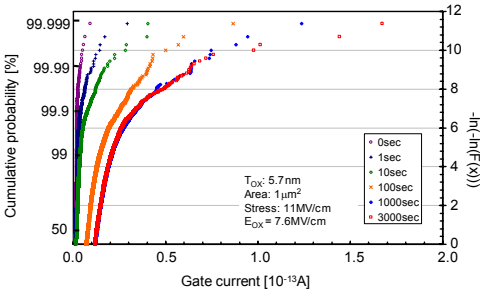


Fig. 7 Distribution of gate leakage current for w/o stress and with stress.

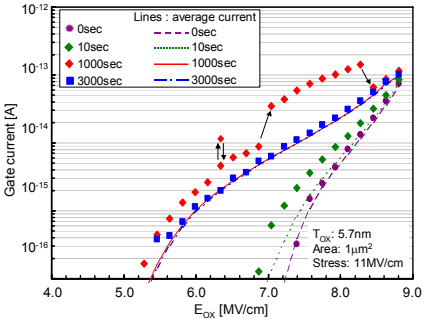


Fig. 8 I_G-V_G characteristic with and w/o stress. With 1000s stress, RTS appeared.

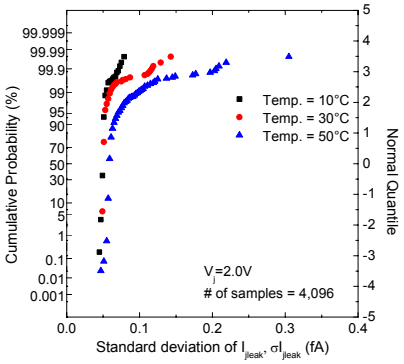


Fig. 9 Temperature dependence of σI_{jleak} distribution.