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A 65nm CMOS 400ns Measurement Delay NBTI-Recovery Sensor by Minimum Assist Circuit

Takashi Matsumoto[1], Hiroaki Makino[1], Kazutoshi Kobayashi[2] and Hidetoshi Onodera[1,3]
[1] Department of Communication and Computer Engineering, Kyoto University, Kyoto, Japan
[2] Department of Electronics, Kyoto Institute of Technology, Kyoto, Japan, [3] JST CREST, Kyoto, Japan
Phone: +81-75-753-5335, Email: tmatsumoto@vlsi.kuee.kyoto-u.ac.jp

1. Introduction

Designing reliable systems becomes more difficult in recent years. Besides conventional problems such as transistor leakage, degradation and variation of transistor performance have severe impact on the dependability of VLSI systems[1]-[3]. In this paper, we deal with negative bias temperature instability (NBTI) which is one of the strongest reliability concerns for digital and analog CMOS circuits[4]-[14]. Especially, we focus on a sensor circuit design which has high fidelity to NBTI recovery monitoring. In the following, first, we clarify the limitation of NBTI recovery measurement by a single PMOS transistor. Then we describe a NBTI-recovery sensor by minimum assist circuit achieving 400ns measurement delay.

2. NBTI-Recovery Measurement by Single PMOS

Fig. 1 shows the typical NBTI recovery measurement result by off-leak current of a single PMOS transistor, where gate bias of stress phase is 2.0V. It is done by an up-to-date semiconductor parameter analyser and 30ms is the fastest initial measurement time in the case of off-leak current measurement. We clearly see step-like recovery behavior. Such kind of step-like behavior is due to individual recovery of positively-charged defects. Recovery starts immediately (generally, at least 1μs) after stress is removed or relaxed. So the minimum measurement delay of 30 ms is too slow to avoid NBTI recovery. As a result, there is an unknown region as shown in Fig. 1, and clarifying the recovery behavior in this region is very important for NBTI recovery modeling. In the next section, we propose a NBTI-recovery measurement circuit which can measure the recovery behavior as short as 400ns initial delay.

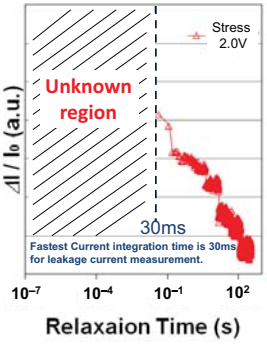

Figure 1: NBTI recovery measurement result by off-leak current of a single PMOS transistor for gate stress bias of 2.0V. The fastest measurement delay is 30ms.

3. NBTI Sensor by Minimum Assist Circuit

Parallelizing many PMOS devices can amplify the off-leak current while achieving high-resolution. But large amount of charge is stored at the drain node of DUT PMOS during the NBTI stress phase. As a result, the measurement range of the analyser changes due to this large injection current, which makes the measurement speed slower. To avoid this problem, we proposed a circuit, which has just two assist NMOSes (MN1 and MN2 in Fig. 2), added to the PMOS DUT. Fig. 2 shows the concept of the proposed circuit. Immediately after the NBTI stress is removed, the charge at node P (drain of DUT) is discharged by MN2 for about 30ns. Then the off-leak current of DUT is measured by opening MN1. These two NMOSes achieves 400ns measurement delay as shown in the next section. Fig. 3 shows the top structure of the proposed circuit. M×N cells in Fig. 2 are connected and the off-leak current of all these cells are measured at the same time. It enables 400ns measurement delay much shorter than single PMOS case (30ms). Fig. 4 shows the unit cell shown in Fig. 2 and the timing chart of the circuit of Fig. 3. The input voltage, VST1, determines whether the DUT is in a stress or recovery mode. Immediately after the DUT enters the recovery mode, VSH becomes "high" for a very short time (about 30ns) to discharge node P in Fig. 4. Due to this discharge, large amount of charge at node P stored during stress mode is not injected to ammeter enabling 400ns measurement delay.

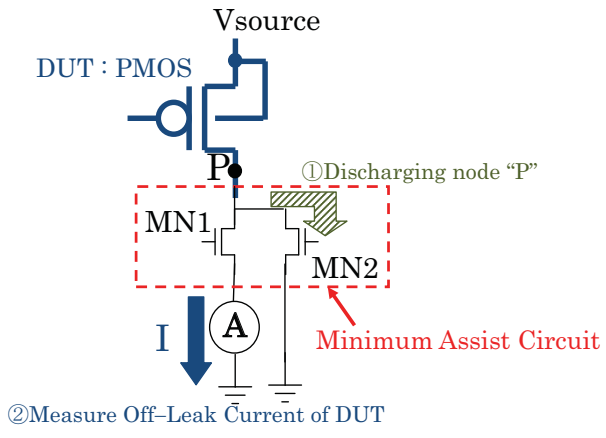

Figure 2: Unit cell circuit constructed from a PMOS DUT and two assist NMOSes.

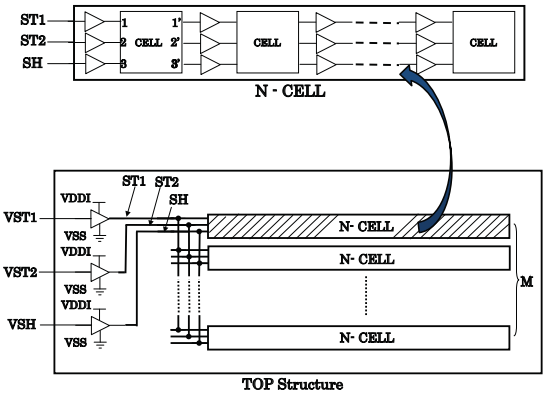

Figure 3: Whole measurement circuit (M×N DUTs).

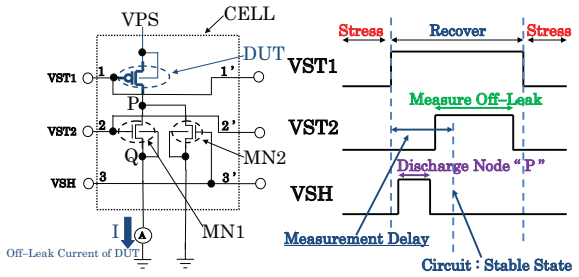

Figure 4: Timing chart of Fig. 3.

VST2 determines the PMOS leakage measurement duration. As shown in Fig. 4, the measurement delay of the circuit depends on the time till the circuit stays in a stable state after VST1 becomes "high". As the number of DUT, namely M×N, increases, the measurement delay also increases. It is 400ns in the case of M=4 and N=540 as shown in the next section. It can also avoid channel hot carrier injection (HCI) during NBTI measurement because all DUTs are in the off state. Fig. 5 shows the chip micrograph. It was fabricated in a 65nm CMOS technology.

4. Measurement Results of Proposed Circuit

Fig. 6 shows the measurement results of NBTI recovery of 2160 PMOS DUTs (M=4 and N=540) after 1000s stress. The horizontal axis is log scale and the vertical axis is linear scale. After one sample is stressed at one temperature for 1000s, it is recovered for 3000s for the same temperature. The temparature is varied from 50°C to 125°C. The measurement delay as defined in Fig. 4 is 400ns. It can measure the unknown region in Fig. 1. NBTI recovery clearly follows log t from 400ns to 3000s for all temperatures. This is because the time constants of positively charged defects are log-uniformly distributed in the PMOS

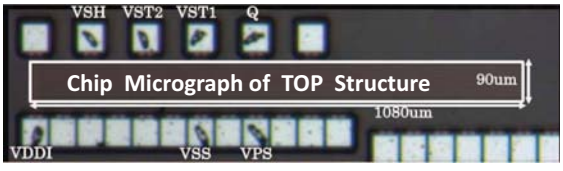

Figure 5: Chip micrograph fabricated in a 65nm CMOS.

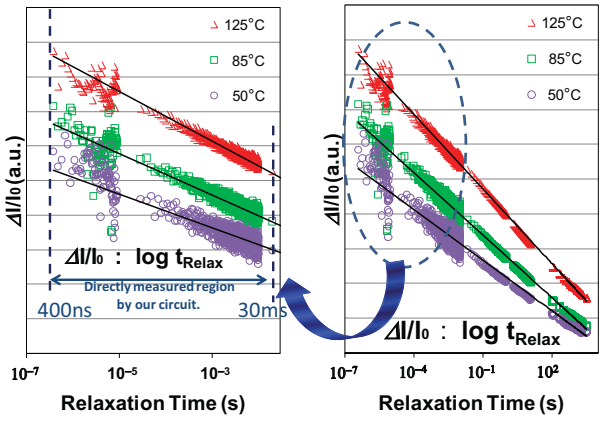

Figure 6: NBTI recovery measurement by the proposed circuit. NBTI recovery follows log t from 400ns for all temperatures. Fitting lines (log t) to the experimental data are also shown.

devices. What we observe in Fig. 6 is an *averaged* recovery behavior of 2160 PMOS transistors connected in parralel. We can observe such a log t behavior without measuring many single transistors individually. During DUT is under the recovery mode, they are all in the off state. So there is no perturbation to the gate bias of DUTs. This enables high-fidelity NBTI recovery measurement, and other conventional methods do not have such a high fidelity.

5. Conclusions

We proposed a NBTI-recovery sensor with 400ns measurement delay which consists one PMOS DUT and two assist NMOSes. It is confirmed that NBTI recovery follows log t from 400ns to 3000s. By degrading and recovering thousands of PMOS transistors at the same time, we can observe that the time constants of positively charged defects which are related to NBTI are log-uniformly distributed in the PMOS devices. Also this circuit has the highest fidelity to NBTI recovery measurement.

Acknowledgement

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