Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp808-809

Prediction of Circuit Degradation with Transient BTI and HC Simulations

Daisuke Hagishima[1], Takamitsu Ishihara[1], Kazuya Matsuzawa[1], and Kazunori Masuda[2]

[1]Advanced LSI Laboratory, [2]Semiconductor Company, Toshiba Corporation
8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan
Tel: +81-45-776-5949, Fax: +81-45-776- 4106, Email: daisuke.hagishima@toshiba.co.jp

1: Introduction

Simulations of the circuit reliability are taking the essential role in the circuit design since the aggressive CMOS scaling degrades the reliability of transistors in terms of as bias temperature instability (BTI) and hot carrier (HC) [1]. The simulations predict the circuit characteristics incorporated with the transistor degradations. However the conventional methods [2] [3] substantially overestimate the degradations because the degradations are extrapolated based on circuit characteristics at the fresh condition without the reduction of the effective stress voltage due to the degradations. We have developed the circuit simulation coupled with dynamic transistor degradations. Self-consistent calculations between the circuit characteristics and the transistor degradations have the advantage of predicting the circuit lifetime. This paper shows that our scheme reproduces measurements of ring-oscillator circuit and is applicable to various circuits.

2: Transient BTI and hot carrier simulations

Fig.1 shows a simple example of the comparison of our scheme with the conventional method for 10-stage buffer circuit. For the conventional method, the delay time of output waveform is 20% worse than for our scheme. This result has a close correlation with the difference in ΔVth of pFETs between the two simulation methods. Fig.2 shows ΔVth of pFET in the 1st stage buffer. The conventional method predicts ΔVth 20% larger than our scheme. Since the circuit simulation is performed coupled with the transient BTI and HC simulations, the effective stress voltage is reduced owing to the transistor degradations in our scheme. Fig.3 illustrates the schematic simulation method to reproduce the characteristics of the degraded MOSFETs. ΔVth(t) and $\Delta I_D(t)/I_D(0)$, current reduction ratio, are incorporated in the circuit simulation. ΔVth(t) and $\Delta I_D(t)/I_D(0)$ are expressed as power low functions extracted from the experimental results of single MOSFETs under DC stress conditions. $\Delta I_D(t)/I_D(0)$ is converted into the gate voltage shift divided by gm, transconductance. The converted $\Delta I_D(t)/I_D(0)$ and ΔVth(t) are assembled into ΔV(t). The characteristics of the degraded MOSFETs are reproduced by appending a time-variable voltage source corresponding to ΔV(t) to the gate. The self-consistent iteration between the circuit simulation and the calculation of ΔVth(t) and $\Delta I_D(t)/I_D(0)$ is a crucially important method for predicting the characteristics of degraded circuits accurately.

3: Impact of circuit configurations on degradations

We have conducted a reliability simulation of 23-stage ring oscillator (Fig.4) for the evaluation of the reproducibility. MOSFETs are fabricated in the conventional process and they have large gate length and thick gate oxides. t_P, the output waveform period (illustrated in Fig.5) is measured at $V_{DD}=V_{MES}$ after the circuit operates at $V_{DD}=V_{STR}$ and 125°C, where $V_{STR}>V_{MES}$. Fig.5 shows simulation and experimental results. The simulation reproduces the time-variation of t_P and its temperature dependence. Fig.6 and Fig.7 show ΔVth of MOSFETs at 85°C and 25°C respectively. HC dominantly degrades n/pFETs at both temperatures. On the other hand, though BTI degrades MOSFETs at 85°C, it has less impact on the circuit at 25°C. Even if the digital circuits have different configurations, they could achieve the same circuit functions. Fig.8 illustrates a shift register circuit configured with D-FF (Fig.8-a). D-FF consists of two D-latch circuits (Fig.8-b) and D-latch is also configured with NOR-logic (Fig.8-c) or NAND-logic circuit (Fig.8-d). Each type of D-latch circuit includes 55 nFETs and 55 pFETs. We have conducted the reliability simulations for all the MOSFETs in both circuits and examined the influence of the circuit configuration on the reliability. Fig.9 shows input and output waveforms at the fresh condition and 125°C. Our scheme indicates the fragile devices in the circuits. NBTI for pFETs is a dominant degradation factor in this condition and Fig.10 shows the three worst and the three best of ΔVth of pFETs in both circuits after 15years of-operation. In addition, Table.1 illustrates the position of the degraded pFETs listed in Fig.10. pFET2 is degraded more than pFET1 in NOR-logic shift register circuit. The simulation results indicate that the circuit configuration has less impact on ΔVth of each MOSFETs, since the configuration of NAND-logic circuit is similar to that of NOR-logic circuit. On the other hand, the delay in the output waveforms is different between the two circuits. As shown in Fig.11, the output waveform of NAND-logic shift register is delayed four times greater than that of NOR-logic shift register. The difference of the circuit robustness between them depends on the stress temperature shown in Fig.12. In terms of the circuit reliability, it is reveled that the shift register with NOR-logic is superior to that with NAND-logic.

4: Conclusions

We developed the circuit simulation coupled with transient BTI and HC simulations. Our simulation reproduces the experimental results and is applicable to various circuits. In addition, it is revealed that the circuit configuration has influence on the circuit reliability even if the circuits have the same functions. Our new scheme has the advantage of simulating the circuit characteristics to reduce excessive quality and design robust VLSI circuits.

References:

[1] M.A. Alam, et.al, Microelectron. Reliab., vol.45, p.71, Jan., 2005 [2] R.H.Tu, et.al, IEEE Trans. Computer-Aided Design, vol.12, p.1524, Oct., 1993 [3] X. Li, et.al, IEEE Trans. Device Mater. Reliab., vol.6, June. 2006

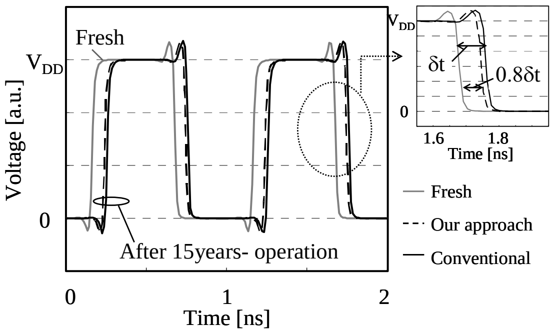


Fig.1. Output waveforms of 10stage-buffer circuit after 15-years operaiton simulated by our scheme and t he conventional method. The inset is an englarged view near the falling edge.

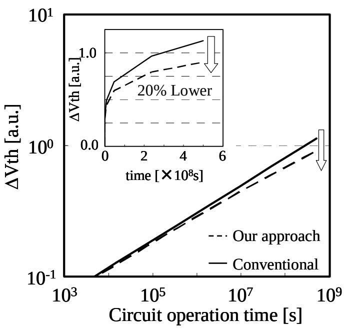


Fig.2. ΔVth of pFET in the 1st-stage of 10stage-buffer circuit. The inset shows linear-linear plot.

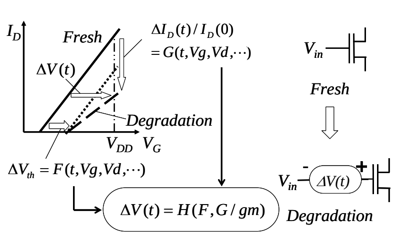


Fig.3. Simulation method to reproduce the charcteristics of degraded MOSFETs in our scheme. ΔV(t) is appended to the gate as a time-variable voltage souce.

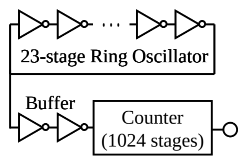


Fig.4. Schematic view of 23stage-ring oscillator. The Ring oscillator and the buffer are intend for the simulation.

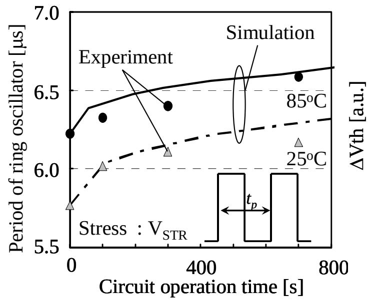


Fig.5. Simulation and experimental results on t_p, output waveform period, of the ring oscillator.

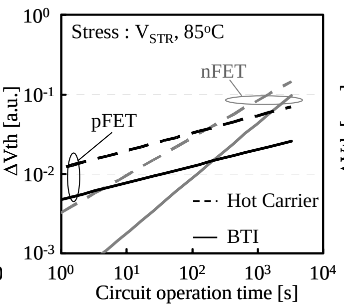


Fig.6. Caluculated ΔVth of MOSFETs in the ring oscillator (V_{STR} and 85°C).

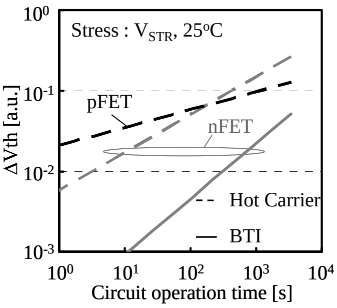


Fig.7. Caluculated ΔVth of MOSFETs in the ring oscillator (V_{STR} and 25°C).

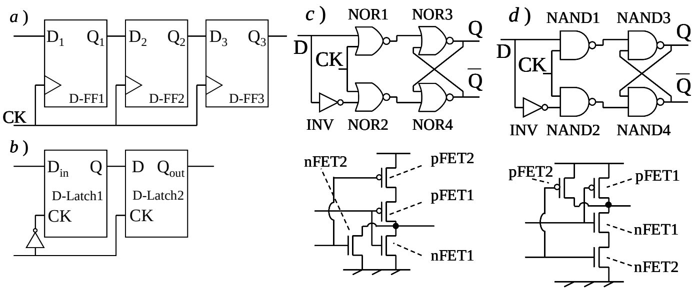


Fig.8. Schematic view of (a) shift register confiured by D-FF, (b) D-FF circuit by D-latch. D-latch consits of (c) NOR-logic or (d) NAND-logic circuit. All the MOSFETs are named for identification.

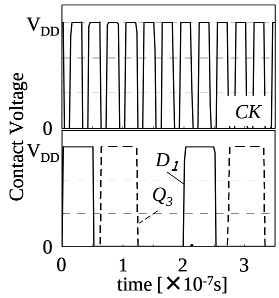


Fig.9. Input (CK and D_1) and output (D_3) waveforms at the fresh condition.

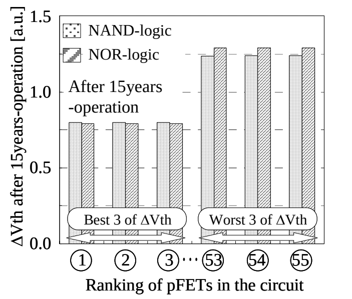


Fig.10. Three worst and best ΔVth(t) of pFETs in the two shift registers. The details of pFETs are shown in Tabel.1

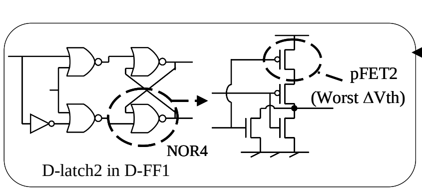
Table.1 The position of pFETs listed in Fig.10.

Details of pFETs in NAND based shift register

Name	①	②	③	53	54	55
pFET in NAND	pFET1	pFET1	pFET1	pFET1	pFET1	pFET1
NAND in D-Latch	NAND3	NAND3	NAND3	NAND1	NAND4	NAND4
D-Latch in D-FF	D-Latch2	D-Latch2	D-Latch2	D-Latch2	D-Latch2	D-Latch2
D-FF in circuit	D-FF3	D-FF2	D-FF1	D-FF3	D-FF2	D-FF3

Details of pFETs in NOR-logic shift register

Name	①	②	③	53	54	55
pFET in NOR	pFET1	pFET1	pFET1	pFET2	pFET2	pFET2
NOR in D-Latch	NOR2	NOR2	NOR2	NOR4	NOR4	NOR4
D-Latch in D-FF	D-Latch2	D-Latch2	D-Latch2	D-Latch2	D-Latch2	D-Latch2
D-FF in circuit	D-FF1	D-FF4	D-FF2	D-FF2	D-FF4	D-FF1



Name of each pFETs and cricuits are reffered in Fig.8. Bottom figure shows the worst degraded pFET in NOR-logic shift register.

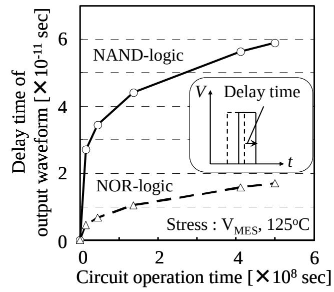


Fig.11. Time variation in the delay time of output waveforms of the both type shift register circuits. The stress condition is V_{DD}=V_{MES} and 125°C.

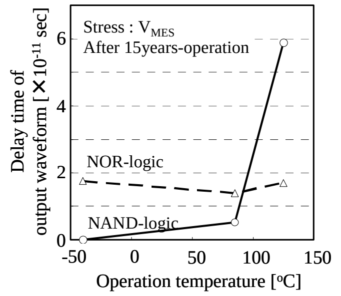


Fig.12. Dependence of the delay time of output waveforms on the stress temperature, where the stress voltage is V_{DD}=V_{MES}.