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A Gate-drain Coupling Distributed Amplifier in 90-nm CMOS Technology

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1. Introduction

Wideband amplifiers are of great interest in various applications [1]-[2]. For wideband communication systems, amplifiers with a large bandwidth are required to achieve high data-rate signal transceiving [2]. Different approaches have been proposed for wideband amplifier design [1]-[7] such as feedback amplifier, travelling-wave amplifier, distributed amplifier, and tuned amplifier with different peaking techniques. The distributed amplifier (DA), using the concept of artificial transmission line, can easily achieve a large bandwidth. However, compared with other wideband amplifier configurations, the DA topology in general has relatively large power consumption and also requires a large chip area. The low efficiency of the DA topology is mainly due to the gain of each stage is added together instead of being multiplied in the multi-stage structure [7]. The large chip area is because of the distributed natural with the long transmission lines for signal traveling.

In this work, we propose a design technique using the transformer coupling between the gate line and drain line in distributed amplifier to achieve a high gain-bandwidth product while maintaining low power consumption. The feedback, realized by the transformer, allows reuse of the traveling signal in a DA and greatly enhances the circuit performance. The transmission lines are employed for the transformer design with the pattern ground shield [1] to minimize the chip size and reduce the insertion loss with a well-controlled coupling factor. Under a power consumption of 60 mW, the proposed design, in 90-nm CMOS, demonstrates a gain-bandwidth product up to 137 (7 dB of gain with a bandwidth of 61.3 GHz) based on the measured results. The measured noise figure is below 6.2 dB up to 40 GHz (frequency range limited by the equipment). The overall chip size is only 1.11×056 mm^2 (core area: 0.97×042 mm^2).

2. Distributed Amplifier with Transformer Feedback

Fig. 1 shows the circuit topology of the proposed distributed amplifier. As illustrated, the gain block of each stage is in a cascode configuration with a peaking inductor L_m connected between the drain of the common-source stage and the source of the common-gate stage to improve the gain-bandwidth product [5]. In addition, the gate and drain lines are coupled through a transformer. In conventional DA design, the gate line and the drain line are connected to the input and output of each stage independently. The signals also travel individually and if the delays of the input/output transmission lines are made equal, the output signal from each individual gain stage is added in phase resulting in wideband characteristics.

Differing from the conventional design, the signals propagating in the gate line and drain line are coupled through the transformer in the proposed design. With the feedback coupling, the signal of the previous stage can be reused from the drain line back to the gate line, and the signal can be amplified again. The amplification efficiency is enhanced and consequently less DC power is needed. Fig. 2 compares the simulation results under two cases. With the identical basic structure, one is the typical DA using the cascode gain stage, and the other is the proposed design with additional transformer feedback. As can be seen, the bandwidth is improved by 50% (from 42 GHz to 63 GHz) with the proposed gate-drain coupling configuration. It is clear that the proposed coupling feedback structure can efficiently improve the gain-bandwidth of the distributed amplifier.

3. Circuit Design and Layout Considerations

As mentioned early, another main issue for DA design is the relatively large chip area. It is critical to have a well-considered floor plan for both the transistors and the gate/drain transmission lines to achieve a compact layout design. In previous reported CMOS DAs [2]-[4], the gate/drain lines and peaking inductors are often designed by spiral inductors. This makes the layout arrangement difficult leaving a large unused chip area. Fig. 3 shows the layout of the gate/drain lines (L_g and L_d) and also the peaking inductor L_m in the proposed design. With the folded topology, the area is greatly reduced. The two sections of proximate transmission lines in the folded structure also function as the transformer feedback. The amount of coupling factor, around 0.15 in every stage of this design, can be determined precisely by the length and distance of the two sections of lines. Note the inductors L_d and L_g can be connected to the transistor directly to minimize the loss of unnecessary interconnects, and hence the chip area is also reduced.

It should be emphasized that the pattern ground shield technique [8] is adopted here to improve the quality factor of the transmission-line inductors. The ground shield can reduce the parasitic capacitance to the ground, and also the reverse current of the substrate. The increase of the effective dielectric constant also reduces the chip area. The peaking inductor L_m, shielded by the Metal 1 layer with a 1-μm width and the interval of also 1μm, is 0.1 nH at 60 GHz. With the pattern ground shield, the EM simulation suggests that the quality factor can be improved by ~ 25%. For the transformer coupling, as indicated by the dotted-line area in

Fig. 3, the pattern ground lines for shielding are rotated by a 90-degree angle to ensure the shielding line is perpendicular to the signal direction to reduce the leakage current to ground and enhance the coupling between gate line and drain line in this region.

4. Measurement Results and Discussion

The proposed gate-drain coupling distributed amplifier was design and fabricated by 90-nm CMOS technology. Fig. 4 shows the chip photograph and the overall chip area is 1.11×0.56mm^2 with a core area of only 0.97×042 mm^2. The S-parameters were measured on-wafer by Aglient E4440A network analyzer from 10 MHz ~ 67 GHz. Fig. 5 shows the measured and simulated S_{21} and S_{12} under the bias condition of V_d=2.2 V, V_m=1.5 V, and V_g=0.66 V, and the corresponding power consumption is only 60 mW. The gain and 3-dB bandwidth of the distributed amplifier is 7 dB and 61.3 GHz. Fig. 6 shows the measured noise figure compared with the simulation. The measured noise figure ranges from 3.8 dB to 6.2 dB in 3 GHz ~ 40 GHz, and the P_{1dB} and IIP3 at 40 GHz are -6.5 dBm and 3.9 dBm, respectively. Table I summaries the circuit performance and also the comparison with prior arts. As can be seen, the proposed distributed amplifier has the lowest power consumption with a small chip area. The achieved FOM is among the best compared with other works listed in the table.

5. Conclusion

This work proposed a gate-drain coupling distributed amplifier using 90-nm CMOS technology. By the gate-drain transformer coupling, the signal was reused and the power consumption was reduced significantly while maintaining a large gain-bandwidth product. The gate/drain lines were arranged in a folded manner with the shielded ground to minimize the chip size. The proposed amplifier demonstrated a gain-bandwidth up to 137.2 GHz under a power consumption of only 60 mA.

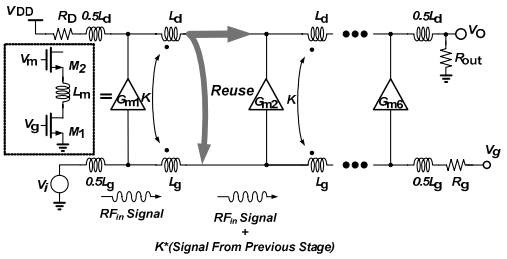

Fig. 1 Proposed distributed amplifier topology.

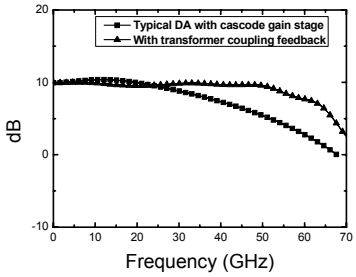

Fig. 2 Bandwidth comparison: with and without gate-drain feedback.

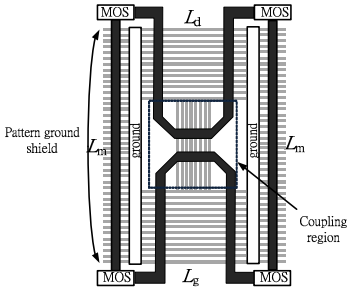

Fig. 3 Layout of the gate/drain lines with feedback.

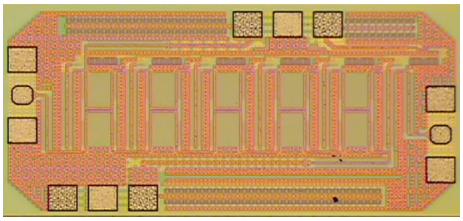

Fig. 4 Chip micrograph of the proposed DA.

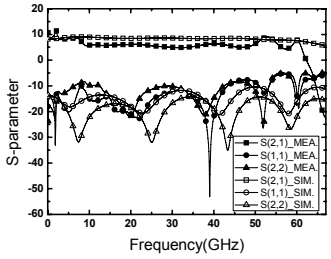

Fig. 5 Measured and simulated S-parameters.

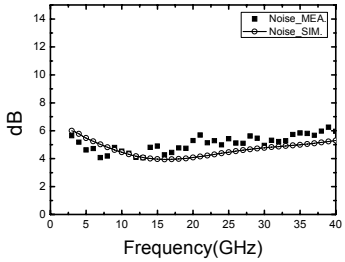

Fig. 6 Measured and simulated of noise figure.

Table I Performance Comparison with Prior Arts

	S_{21} (dB)	BW (GHz)	GBW (GHz)	Power (mW)	Size (mm^2)	FOM	Process
This design	7	61.3	137.2	60	0.62	36.9	90 nm CMOS
[2]	9.8	44	136	103	1.5	14.7	0.13 μm CMOS
[3]	20	39.4	394	250	2.24	14.1	0.18 μm CMOS
[5]	9.5	32	96	97	0.81	24.3	0.18 μm CMOS
[6]	7.4	80	187	120	0.72	21.7	90 nm CMOS

$$FOM = 1000 \cdot \frac{GBW}{P_{dc} \cdot f_t \cdot Area}$$

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