Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp812-813

A 60dB SFDR Low-Noise Amplifier with Variable Bandwidth for Neural Recoding Systems

Katsuya Sueishi[1], Takeshi Yoshida[1], Atsushi Iwata[2],
[3]Kojiro Matsushita, [3]Masayuki Hirata, [4]Takafumi Suzuki

[1]Graduate School of Advanced Sciences of Matter, Hiroshima University
1-3-1 Kagamiyama, Higashihiroshima-shi, Hiroshima 739-8530, Japan
[2]A-R-Tech Corporation
[3]Department of Neurosurgery, Osaka University Medical School
[4]Graduate School of Information Science and Technology, Tokyo University
E-mail: sueishi@dsl.hiroshima-u.ac.jp

1. Introduction

Recently, a brain machine interface (BMI) /brain computer interface (BCI) has been researched in order to restore communication function for the severely disabled people due to amyotrophic lateral sclerosis, spinal injury, brain stroke etc. Especially, Electrocorticograms (EcoG) is attracting attention as a key signal to realize these systems.

The EcoG has a signal bandwidth of 0.1Hz to 100Hz, and signal amplitude of a few μV to 1mV. Thus the low-noise amplifier for the EcoG detection should have an input referred noise of a few μV to detect accurately the signal with low frequency and small amplitude. Moreover, the low-noise amplifier requires a control of the signal bandwidth and a high dynamic range because the EcoG detection and unwanted noise such as induced noise of AC power supply are input simultaneously. In this paper, a low-noise amplifier for the EcoG detection is proposed. The proposed amplifier achieved high linearity and wide variable range of signal bandwidth by using a resistor of the subthreshold-biased cascade MOSFETs with a few TΩ.

2. High-Value Resistance MOSFET for Low Noise Amplifier

A subthreshold-biased MOSFET as a feedback resistor with a high resistance is widely used for biosignal amplifier to amplify low frequency signal [2,3]. However, it is possible to use the subthreshold-biased MOSFET with a high resistance while the gate-source voltage Vgs and the drain-source voltage Vds of the MOSFET are small. When the output voltage swing of the biosignal amplifier will be large, a resistance value of the feedback resistor implemented by the MOSFET changes greatly and then it causes the deterioration of linearity. In case of adjusting low roll-off frequency of the amplifier using the gate voltage VG, the linearity of the amplifier is worse. Thus it is necessary to suppress the degradation of linearity.

3. Circuit Architecture and Low-Voltage Design

The schematic of a low-noise amplifier is shown in Fig. 1. The low-noise amplifier consists of a fully-differential opamp, AC coupled capacitors Cin, feedback capacitors Cf and feedback resistors Rf implemented by cascade MOSFETs, thus the low-noise amplifier realize high input impedance and a high-pass filter characteristic. A roll-off frequency of the high-pass filter is determined by both the Rf and the Cf. In case of a 0.18-μm CMOS technology, a capacitance value of the Cf, which is limited by parasitic components and characteristic deviation, is 50fF. To achieve less than 0.01Hz of low roll-off frequency, the resistance of Rf needs more than 318 TΩ. Thus the Rf is implemented by cascade MOSFETs operated in subthreshold. In addition, a wide variable range of bandwidth is accomplished with adjusting the VG of MOSFET.

Figure 2 shows the schematic of the fully-differential opamp in the low-noise amplifier. To achieve a high voltage gain and wide output swing, folded-cascode opamp is used. Moreover, 1/f noise is decreased by enlarging the area of M2 and M3 that is the major factor of 1/f noise.

4. Experimental Results

A chip micrograph of the low-noise amplifier fabricated by a 0.18-μm CMOS technology is shown in Fig. 3. The measured frequency response is shown in Fig. 4. The proposed amplifier achieved a variable bandwidth from 0.04Hz to 30Hz by adjusting the VG from 0.75V to 1V. A voltage gain can be set from 28dB and 40dB as shown in Fig. 5. The measured SFDR versus output amplitude at VG=0.85V is shown in Fig. 5. Figure 5 compares the SFDR of cascade connected 12-MOSFETs with that of a MOSFET. In case of the cascade connected 12-MOSFETs, the amplifier achieved more than 60dB SFDR when defining 0.2Vpp output swing. The SFDR is improved about 20dB compared with a MOSFET. Moreover, the amplifier with the cascade connected 12-MOSFETs achieved more than 40dB SFDR when defining 0.6Vpp output swing. Thus the proposed amplifier with the cascade connected 12-MOSFETs can control low roll-off frequency range of triple-digits with maintenance of a high linearity. Figure 6 shows measured input referred noise. The input referred noise in the signal bandwidth is 2.5μVrms.

5. Conclusions

Low-noise amplifier with high dynamic range and wide variable range of bandwidth is proposed. When defining 0.2Vpp output swing, the proposed amplifiers with a feedback resistor of cascade connected 12-MOSFETs operated in the subthreshold achieved a variable low roll-off frequency of 0.04Hz~30Hz and more than 60dB SFDR. The input referred noise is 2.5μVrms.

Acknowledgements

This work was supported in part by the Strategic Research Program for Brain Sciences of MEXT, Grants-in-Aid for Scientific Research (20300199) from JSPS. The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

References

[1]T. Denison, K. Consoer, A. Kelly, A. Hachenburg, and W. Santa, "A 2.2μW 94nV/√Hz, Chopper-Stabilized Instrumentation Amplifier for EEG Detection in Chronic Implants," ISSCC Dig. Tech. Papers, pp. 162-163, 2007.

[2] X. Y. Xu, X. D. Zou, L. B. Yao, and Y. Lian, "A 1-V 450-nW Fully Integrated Biomedical Sensor Interface System," 2008 Symp. VLSI Circuits Dig. Tech. Papers, pp. 78-79, 2008.

[3] R. R. Harrison and C. Charles, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications," IEEE J. Solid-State Circuits, pp. 958-965, Jun.2003.

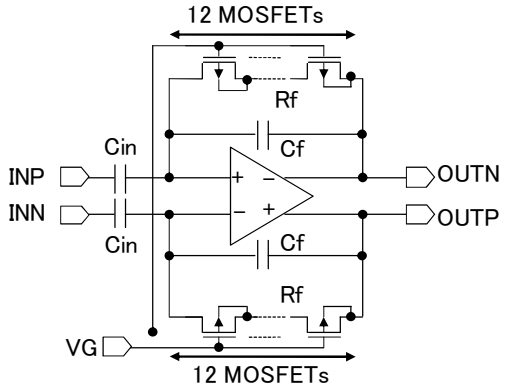

Fig.1 A circuit of low-noise amplifier.

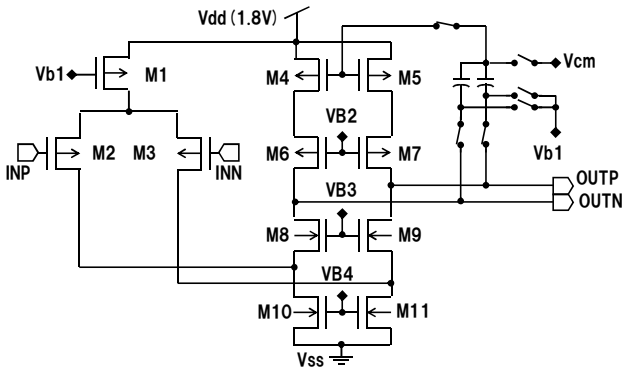

Fig.2 Schematic of the fully-differential opamp.

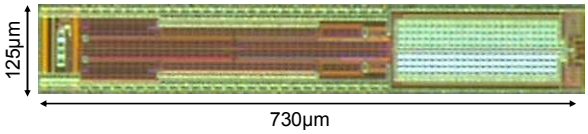

Fig.3 Chip micrograph.

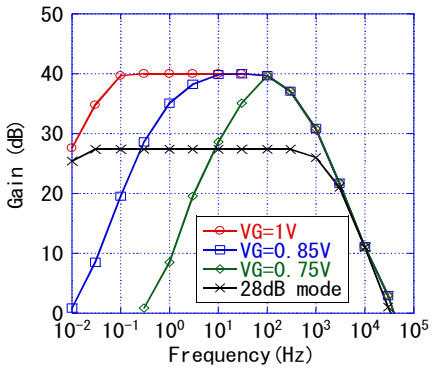

Fig.4 Measured frequency response.

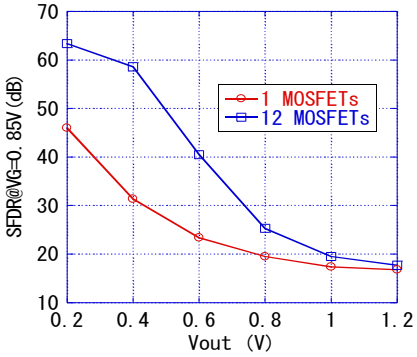

Fig.5 Measured SFDR vs. output amplitude at VG=0.85V.

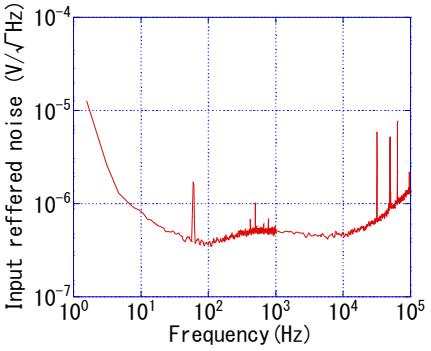

Fig.6 Measured input referred noise.

Table 1 Performance Comparison.

Parameter	Ref[1]	Ref[2]	Ref[3]	This work
Supply voltage	1.8V	1V	±2.5V	1.8V
Process technology	0.8μm CMOS	0.35μm CMOS	1.5μm CMOS	0.18μm CMOS
Current	1.2μA	337nA	180nA	10.4μA
Midband gain	45.5dB(tunable)	60dB(tunable)	39.8dB	40dB(tunable)
High-pass f_{-3dB}	0.5Hz(tunable)	0.5Hz(tunable)	0.014Hz	0.1Hz(tunable)
Low-pass f_{-3dB}	250Hz(tunable)	292Hz(tunable)	30Hz	100Hz
Input referred noise	0.93μV (0.5~100Hz)	2.5μV (0.05~460Hz)	1.6μV (0.5~30Hz)	2.5μV (0.1~100Hz)
CMRR	105dB	71.2dB	86dB	76.9dB
PSRR	–	84dB	80dB	86dB
THD	–	<0.6% (at 1Vpp output swing)	<1% (at 1.2Vpp output swing)	<1% (at 1Vpp output swing)
Area	1.4mm^2	0.64mm^2	0.22mm^2	0.09mm^2