Temperature Compensated Nano-Ampere CMOS Current Reference Circuit Using Small Offset Voltage

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1. Introduction

We developed a low-power current reference circuit with little temperature dependence for micro-power LSIs in a 0.35-μm standard CMOS process. The proposed circuit consists of a bias-voltage subcircuit, a current-source subcircuit, and an offset-voltage generation subcircuit. The offset-voltage generation subcircuit is used to compensate for temperature dependence of the reference current. Experimental results demonstrated that the proposed circuit generates a 93-nA reference current, and that the total power dissipation is 586 nW. The temperature coefficient of the reference current can be kept small within 459ppm/°C in a temperature range from −20 to 100°C.

2. Circuit Configuration

Figure 1 shows our proposed current reference circuit. The circuit consists of a bias-voltage subcircuit, a current-source subcircuit and an offset-voltage generation subcircuit. All MOSFETs are operating in the subthreshold region except a MOS resistor (MR) operating in the strong-inversion and deep triode region. The proposed circuit is based on the threshold-voltage reference circuit [1]. In [1], current flowing in the circuit is tolerant to process variations and supply voltage change. However, the current shows a positive temperature coefficient and increases with temperature. To realize robust temperature stability, we modify the circuit by using small offset-voltage generation subcircuit. The details of the circuit are as follows.

The subthreshold current I of a MOSFET for drain-source voltage V_{DS} higher than 0.1 V can be expressed as

$$I = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right), \qquad (1)$$

where K is the aspect ratio ($= W/L$) of the transistor, I_0 ($= \mu C_{OX}(\eta-1)V_T^2$) is the process-dependent parameter, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, η is the subthreshold slope factor, V_T ($= k_B T/q$) is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, and V_{TH} is the threshold voltage of the MOSFET [2]. The temperature dependence of the mobility μ can be given by

$$\mu(T) = \mu_0(T/T_0)^{-m}, \qquad (2)$$

where μ_0 is the mobility at room temperature T_0 and m is the mobility temperature exponent [2].

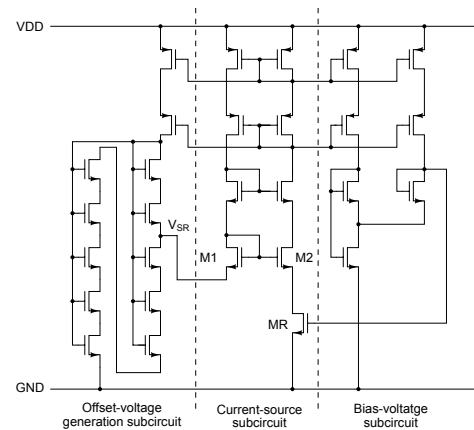In Fig. 1, the current I_{REF} is determined by the characteristics of the MOS resistor MR that is operating in the strong-inversion and deep triode region. When drain-source voltage V_{DSR} is small enough, the current is given by

$$I_{REF} = \mu C_{OX} K_R (V_{GS} - V_{TH}) V_{DSR}. \qquad (3)$$

In our current reference, the offset-voltage generation subcircuit performs a crucial role through the drain-source voltage V_{DSR}.

The offset-voltage generation subcircuit consists of MOSFET resistor ladder. All MOSFETs operate in the subthreshold linear region except the diode-connected transistor which operates in the subthreshold saturation region. Although the internal voltage of V_{SR} in the offset-voltage generation subcircuit can be expressed with a non-linear function, the voltage V_{SR} can be approximated by a linear temperature dependent voltage with a small offset-voltage in the temperature range from −20 to 100°C. The voltage V_{SR} can be modeled by

$$V_{SR} = \gamma T + \beta, \qquad (4)$$

where γ is temperature coefficient of V_{SR} and β is the offset voltage. Note that the temperature coefficient γ and the offset voltage β can be controlled by the number of transistors and the tap point.

From Eq. (4), the drain-source voltage V_{DSR} of MR can be given by

$$\begin{aligned} V_{DSR} &= V_{SR} + V_{GS1} - V_{GS2} \\ &= V_{SR} + \eta V_T \ln(K_2/K_1), \qquad (5) \\ &= \alpha T + \beta \end{aligned}$$

$$\alpha = \gamma + \eta \frac{k_B}{q} \ln(K_2/K_1). \qquad (6)$$

From Eqs. (2), (3), (5) and (6), temperature coefficient of the reference current TC ($= 1/I_{REF} \cdot \partial I_{REF} / \partial T$) is given by

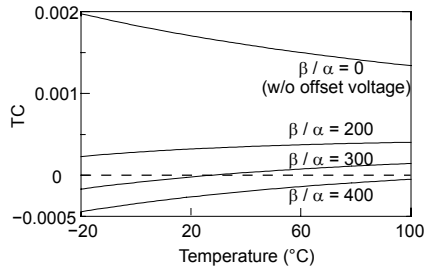Fig. 1　Schematic of proposed current reference circuit.

Fig. 2 Calculated temperature coefficient of the reference current *TC* (Eq. (7)) as a function of temperature with different β/α as a parameter.
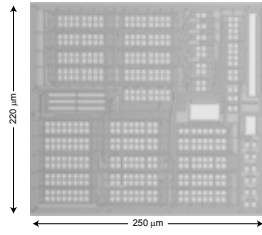

Fig. 3 Chip micrograph.

$$TC = \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{(V_{GS}-V_{TH})}\frac{d(V_{GS}-V_{TH})}{dT} + \frac{1}{V_{DSR}}\frac{dV_{DSR}}{dT}$$

$$= \frac{-m}{T} + \frac{1}{T} + \frac{\alpha}{\alpha T + \beta} \qquad (7)$$

$$= \frac{1-m}{T} + \frac{1}{T+\beta/\alpha}$$

From Eq. (7), considering the range of β/α, the second term will change from 0 to $1/T$. In standard CMOS technology, because *m* is about 1.5 [2], *TC* can be set to 0 at room temperature by designing β/α to an appropriate value. Figure 2 shows calculated *TC* as a function of temperature with different β/α as a parameter. Without an offset voltage ($\beta/\alpha = 0$), *TC* is always positive and the current I_{REF} increases with temperature. With an offset voltage, *TC* can be controlled as shown in Fig. 2. At $\beta/\alpha = 300$, *TC* can be made "0" at room temperature. Therefore, temperature compensated reference current can be obtained by adjusting γ, β, and the aspect ratios of transistors (M1-M2) such that *TC* is equal to "0" at room temperature.

3. Experimental Results

We fabricated a prototype chip using a 0.35-μm, 2-poly, 4-metal standard CMOS process. The subthreshold MOS resistor ladder in the proposed current reference circuit consists of 10 transistors and the tap point is set to 8 as shown in the Fig. 1. Figure 3 shows a chip micrograph of our prototype chip. The area was 0.055mm^2. The power supply voltage was set to 2.5-V.

Figure 4 (a) shows measured internal voltage V_{SR} as a function of temperature from −20 to 100°C. The internal voltage in the offset-voltage generation subcircuit showed positive temperature dependence with a small offset-voltage. The offset voltage was about 7.2 mV.

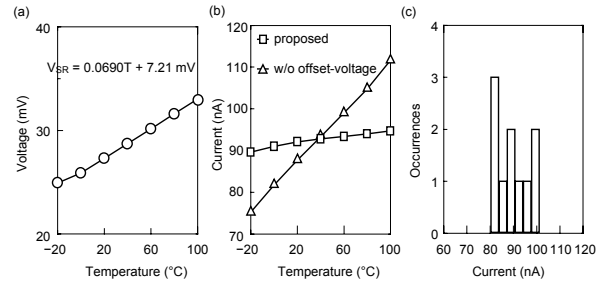Figure 4 (b) shows measured output current I_{REF} as a

Fig. 4 Measured results of (a) the internal voltage V_{SR}, (b) the proposed reference current and the current without using offset-voltage generation circuit, and (c) distribution of the proposed current for 10 samples.

Table I Comparison of reported nano-ampere current references

	This work	[3]	[4]	[5]
Technology	0.35-μm	N/A	0.8-μm	3-μm
I_{REF} (nA)	92.5	287	430	774
Power (nW)	586	N/A	2150	7000
Temp. (°C)	−20-100	0-75	N/A	0-80
TC (ppm/°C)	459	226	6000	375
Min. Supply (V)	1.8	N/A	2.5	3.5
Line reg. (ppm/V)	1710	4000	5000	150

function of temperature from −20 to 100°C. The current that was generated without using the MOS resistor ladder was also shown. While the current without the MOS ladder increased with temperature, temperature dependence of the output current I_{REF} can be made little by using the MOS resistor ladder. The average output current was about 92.5 nA. The *TC* was 459ppm/°C. The circuit operated correctly with a power supply more than 1.8 V, and the line regulation was 1710ppm/V in the supply range of 1.8 to 3 V. A constant reference current with little temperature and power supply dependence was obtained. The total power dissipation was 586 nW with a 1.8-V power supply.

Figure 4 (c) shows the distribution of the measured output current I_{REF} in 10 samples at room temperature. The coefficient variation (= σ/μ, where μ and σ are the mean value and the standard deviation of the output current I_{REF} distribution) was 7.5%.

Table I summarizes circuit performances in comparison with other nano-ampere CMOS current reference circuits [3]-[5]. Compared to the other CMOS current reference circuits, the proposed circuit shows lower power dissipation. The proposed circuit compensates temperature dependence with high process stability. The proposed circuit is useful as a current reference circuit for a micro-power LSIs.

References

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