Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1150-1151

CMOS High-Speed Image Sensors
- Pixel Devices, Circuits and Architectures -

Shoji Kawahito

Shizuoka University
3-5-1 Johoku Naka-ku,
Hamamatsu 432-8011, Japan
Phone: +81-53-478-1313 E-mail: kawahito@idl.rie.shizuoka.ac.jp

1. Introduction

High-speed imaging is one of promising applications for CMOS image sensors. The application of high-speed imaging is spreading to various fields such as scientific, industrial, broadcasting and automobile cameras and consumer products. These applications require high-speed image sensors with both high speed and high image quality.

In this paper, recent progress of CMOS high-speed image sensors is reviewed and discussed from the viewpoints of pixel devices and circuit techniques. An on-chip analog-to-digital converter (ADC) is a key element of the high-speed CMOS image sensor. Column-parallel ADCs are the most promising for power-efficient high-speed high-quality image readouts. Possible column-parallel ADC architectures are compared and discussed. A global electronic shutter is another approach for capturing high-speed moving scene. Recent developments of global shutter pixels for low-noise and high shutter efficiency are discussed.

2. Architecture

Figure 1 shows a typical architecture of high-speed CMOS image sensors. Pixel outputs are read out through column correlated double sampling (CDS), ADC and horizontal readout circuits. The CDS function is often embedded in the column ADC itself, or done in digital domain. The digital-domain CDS, or digital CDS is becoming a popular technique because of its extremely small vertical FPN[1][2][3].

For horizontal readouts, a low-voltage differential signaling (LVDS) is becoming an important technique not only for high-speed readouts but also for low-noise generation because of the differential signal form. This allows us to use pipelined readout operation as shown in Fig. 2.

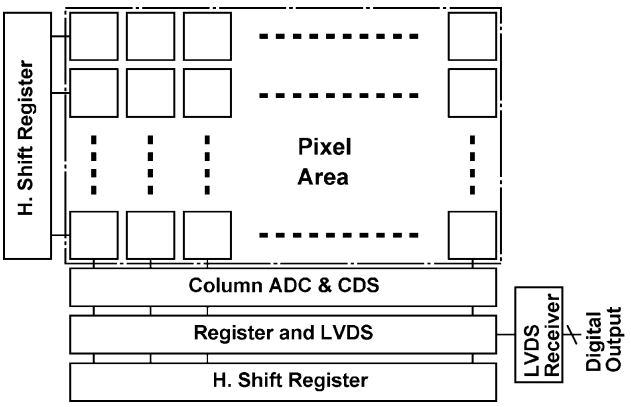

Fig. 1 Architecture of High-Speed CMOS Imagers.

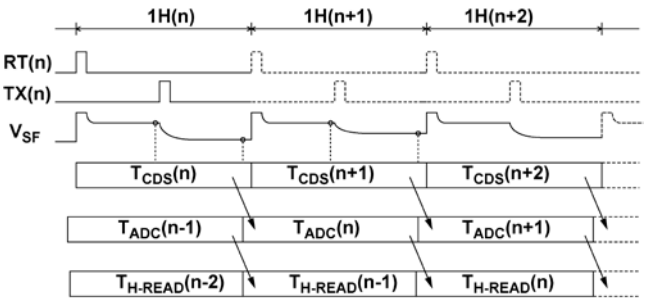

Fig. 2 Pipelined readout operation.

To completely suppress the digital noise due to the horizontal readout operation, the readout operation can be done at different timing from the analog operations of CDS and ADC. However, this is not suitable for high-speed imagers. The horizontal readout using the low-noise LVDS can be done at the background of the analog operation and this accelerates the speed. The ADC can also be done at the background of the CDS operation. However, very careful timing design is necessary to prevent the coupling noise between the CDS and ADC.

3. column-parallel ADC

The most commonly-used column parallel ADC is a single-slope integration type ADC. Fig. 3 shows a single-slope ADC using a hybrid CDS technique. Using a capacitor connected at the pixel output and an auto-zeroing switch for a comparator, an analog CDS is performed for reducing the ADC period for reset level by eliminating the pixel offset [1]. With a ramp signal, the single-slope A/D conversion for reset level is carried out first using down-counting mode of the counter. Then signal level is given at the input of the ADC by transferring signal charge to the floating diffusion of the pixel and the single-slope

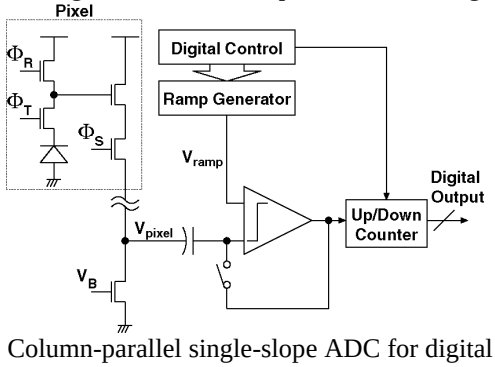

Fig. 3 Column-parallel single-slope ADC for digital CDS.

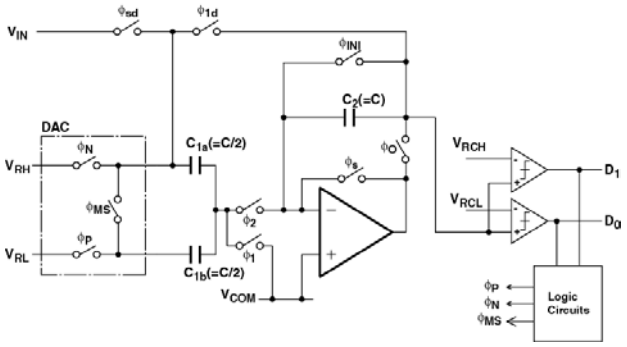

Fig. 4 Column-Parallel Cyclic ADC.

A/D conversion for signal level is performed using up-counting mode of the counter. The difference between up and down counting memorized in the counter corresponds to the digital CDS, and this eliminates effectively the fixed pattern noise caused by the offset of the comparators and clock skew as well as kTC noise. Using high-speed clock of 297MHz, 12-bit resolution has been achieved for 2.8Mpixels at 30frame/s. It can also be operated at 180frames/s for 10-bit resolution.

A column-parallel successive approximation (SA) ADC technique is useful for high-speed CMOS image sensors, since it has higher conversion speed compared to the single-slope integration type. A 8.3Mpixel 60 frames/s CMOS image sensor using column-parallel 10b SA-ADC has been developed [2].

A cyclic or algorithmic ADC is suitable for high gray-scale resolution and high conversion speed since it requires the number of conversion steps of *N-1* for an *N*-bit ADC. Recently, a cyclic ADC with very simplified circuit topology as shown in Fig. 4 is reported [3]. It consists of one operational amplifiers, two comparators, 2 capacitors, and transistor switches. A full 13-bit resolution without any calibration has been achieved in the implementation of 390 frames/s VGS-size CMOS imager. A high-speed version of the cyclic ADC is used for a 512x512-pixel 3500frames/s CMOS image sensor [4].

Table I Comparison of Column ADCs.

ADC	Single Slope	SA	Cyclic
Conversion time (N bits)	△ (2^N x T_{ck})	○ (N x T_{ck})	◎ ((N-1) x T_{ck}, Acceleration possible)
Pixel Pitch (Minimum Reported)	◎ 2.5um(One side)	△ 3.75um (Double Side)	○ 5.6um(One Side) 2.25um(Double Side,2:1Mux)
Resolution	△ (12bit)	○ (14bit)	◎ (14bit, DR=71dB)
Area (analog)	◎ (Comparator)	△ (Comparator, Capacitor Array)	○ (Comparator, Opamp, Capacitors)
Power Consumption	○ (Comparator, Ramp generator, High-Speed Clock)	○ (Comparator, Voltage Reference)	△ (Opamp, Comparator, Voltage Reference)

Comparison of the three types of column ADCs is shown in Table I. The single-slope ADC has an advantage of embedding the ADC in fine pixel pitch. The SA ADC is suitable for high frame rate while maintaining low-power consumption. Because of the capacitor array for the digital-to-analog conversion, it is not always suitable for fine pixel pitch. The cyclic ADC is the fastest and it is suitable for high-resolution. A Delta Sigma ADC is another column-parallel high-performance ADC. A column parallel 2^{nd}-order delta-sigma ADC is used for a 2.1Mpixel 120frame/s CMOS image sensor and a low-noise level of 1.9e- and low-power dissipation of 180mW has been achieved [5].

4. Pixel Technology

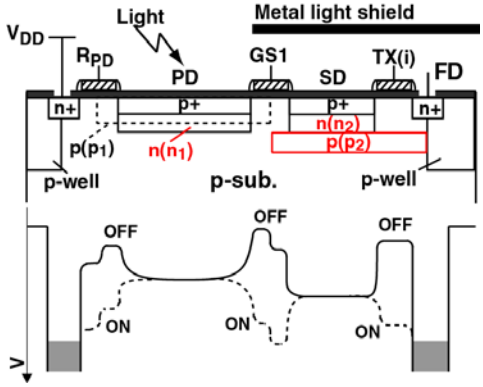

Fig. 5 CMOS active pixel for a low-noise global shutter.

A global electronic shutter pixel is one of the most important functions for high-speed image sensor. While a 5-Tr. global shutter pixel using a floating diffusion memory is widely used for CMOS image sensors, a low-noise global shutter pixel has been required because the 5-Tr. global shutter has high random noise level due to kTC noise. Recently, a very low-noise global shutter as shown in Fig. 5 is presented [6]. The two-stage charge transfer structure using pinned diodes allows us to cancel kTC noise and to attain low-dark current. A low noise level of 2.7e- has been achieved.

5. Conclusions

CMOS image sensors have low-noise performance at high frame rate. Column ADCs and column signal conditioning circuits contribute to it. A problem of noisy global shutters in CMOS imager sensors has been solved by the developments of two-stage charge transfer structure for the global shutter.

Acknowledgements

A part of this work was supported by the Ministry of Education, Culture, Sports, Science and Technology under Grant-in-Aid for Scientific Research (A), No. 19206040, and the Knowledge Cluster Initiative.

References

[1] S. Yoshihara, et al., IEEE J. Solid-State Circuits, **41** (2006) 2998.
[2] S. Matsuo et al., IEEE Trans. Electron Device, **56** (2009) 2380.
[3] J. H. Park, S. Aoyama, T. Watanabe, K. Isobe, S. Kawahito, IEEE Trans. Electron Devices, **56** (2009) 2414.
[4] M. Furuta, Y. Nishikawa, T. Inoue, S. Kawahito, IEEE J. Solid-State Circuits, **42** (2007) 766.
[5] Y. C. Chae, et al., Dig. Tech. Papers, ISSCC (2010) 394.
[6] K. Yasutomi et al., Dig. Tech. Papers, ISSCC (2010) 398.