A Column Parallel Cyclic ADC with an Embedded Programmable Gain Amplifier for CMOS Image Sensors

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1. Introduction

The performance requirements of next-generation CMOS image sensor have been increasing in terms of frame rate, read noise, dynamic range (DR), as well as pixel resolution. In order to meet the requirements of high-speed, low-noise and wide DR, a column readout architecture using and a column programmable gain pre-amplifier and column analog-to-digital converter (ADC) is becoming a popular technique [1][2][3]. However, the use of column PGA leads to the increase of die area and power consumption. Recently the noise level of CMOS image sensors with column ADCs is greatly improved [4][5]. However, without the help of the pre-amplifier, it is not easy to achieve the state-of-the-art noise level of 1 to 3 electrons.

This paper presents a new architecture of a column parallel ADC with an embedded programmable gain amplifier (PGA) for high-speed low-noise wide DR CMOS image sensors. The proposed technique uses a modified cyclic ADC circuit topology where capacitors for cyclic ADC are divided into several small capacitors and the connection of the small capacitors is programmed for embedding a function of the PGA in the ADC. This technique does not much increase the area and power consumption when compared with the straightforward cyclic ADC. A prototype CMOS imager chip is implemented with 0.18um CIS technology and the basic characteristics of linearity and noise of the cyclic ADC with PGA is measured.

2. ADC/PGA Architecture

Fig. 1 shows the schematic diagram of the column parallel cyclic ADC with an embedded PGA. It consists of a single-ended amplifier, capacitors, comparators, switch transistors and control logic circuits. The variable gain of 1, 2, 4 and 8 can be obtained by changing the connection of capacitors with switches. The PGA has a function of correlated double sampling (CDS) of the pixel outputs. After the PGA/CDS operation, the capacitors are connected for the subsequent cyclic A/D conversion.

The phase diagram for the operation of the PGA and subsequent cyclic ADC is shown in Fig. 2. In the PGA/CDS operation, the reset level of the pixel output (V_{RES}) is given at the input and sampled in capacitors C_1 and C_3 while initializing charge in the feedback capacitor C_2 (Fig. 2(a)), and then the signal level (V_{SIG}) is given at the input and the charge stored in C_1 and C_3 is transferred to C_2 (Fig. 2(b)). The resulting amplifier output is given by G ($V_{RES} - V_{SIG}$) where G is the gain given by $G=(C_1+C_3)/C_2$. Therefore, an amplified noise-cancelled signal appears at the output. The cyclic A/D conversion starts from the sampling of



Fig. 1 Cyclic ADC with an embedded PGA.

amplifier output with C_1 and C_3 (Fig. 2(c)). In this phase, the first-cycle sub-A/D conversion is also done. The gain-of-two amplifying digital-to-analog conversion is done as shown in Fig. 2(d). In this amplification phase, C_3 and C_2 are used for the feedback capacitors and C1 is used for D-to-A conversion. The next sampling of the output is done as shown in Fig. 2(e), where the output is sampled by C_1 only. In this sampling phase, sub-A/D conversion is also done. The cyclic or algorithmic A/D conversion is performed by repeating the sampling phase of Fig. 2(e) and the



Fig. 2 Phase diagram for the operation of PGA and cyclic ADC.

amplification phase of Fig. 2(d).

The gain of 1, 2, 4 and 8 can be programmed by choosing the connection of capacitors as shown in Table I.

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G	C ₁	C ₃	C ₂
1	(18C)	-	C ₂₀ +C _{3a} +C _{3b} +C _{3c} (18C)
2	(18C)	C _{3a} +C _{3b} +C _{3c} (6C)	C ₂₀ +C _{3a} +C _{3b} (12C)
4	(18C)	C _{3a} +C _{3b} +C _{3d} (14C)	C ₂₀ +C _{3c} (8C)
8	(18C)	C _{3a} +C _{3b} +C _{3c} (14C)	C ₂₀ (4C)
$[C_{1a}]=[C_{1b}]=9C, [C_{20}]=[C_{3b}]=[C_{3c}]=[C_{3d}]=4C, [C_{3a}]=6C$			

Table I Arrangement of capacitors for programming the PGA.

3. Measurement Results

A microphotograph of the prototype CMOS imager chip implemented with $0.18\mu m$ CMOS image sensor technology is shown in Fig. 3. The imager has a column parallel cyclic ADC with an embedded PGA. The pixel uses 4Tr-based pinned-photodiode active pixel sensor.



Fig. 3 Prototype CMOS imager with column ADC/PGA.

Measured differential nonlinearity (DNL) plot of the ADC is shown in Fig. 4. The master clock used is 20MHz which



Fig. 4 Measured linearity (DNL) of the ADC.

corresponds to 16µs as a horizontal time. The maximum DNL is $\pm 0.2/-0.9$ LSB at 13-b resolution for the case of PGA gain of 1. Though the maximum DNL increases to 1.1LSB for the PGA gain of 8, the input referred value is 0.13LSB. This shows the effectiveness of the PGA for the reduction of ADC non-linearity. Fig. 5 shows the measured random noise as a function of the gain of the PGA. When the gain is unity, the random noise is $218\mu V_{rms}$ and it shows that the random noise can be reduced by increasing the gain. For the gain of 8, the noise level is reduced to $128\mu V_{rms}$. This noise does not include the pixel source follower noise. If this noise level is achieved as the noise of CMOS imager and the conversion gain can be as high as $80\mu V/electron$, the noise level corresponds to 1.6 electrons.



Fig. 5 Input-referred r.m.s. noise as a function of PGA gain.

4. Conclusions

This paper proposes a column parallel cyclic ADC with an embedded programmable gain amplifier. The measurement results of a prototype chip show the effectiveness of the embedded PGA for the reduction of ADC non-linearity and random noise. The evaluation of the performance as a CMOS imager is left as a near future subject.

Acknowledgements

The present study was supported in part by Grant-in-Aid for Scientific Research 19206040.

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