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Qpix v.1: A high speed 400-pixels readout LSI with 10-bit 10MSps pixel ADCs

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1. Introduction

Hybrid semiconductor detectors have become important tools for particle tracing, radiation detecting systems in high energy physics experiments, and fast imaging applications with penetrating radiation [1]. Conventional pixel readout LSI for hybrid detector such as Timepix [2] can measure time of flight (TOF) or time over threshold (TOT). However, the deposited total charge Q is estimated from TOT readings. This method definitely results in unacceptable inaccuracy of total charge measurement, especially in 3D tracking applications, such as vertex detectors [4].

A new architecture readout LSI: Qpix (Quasi-3D Pixel) was proposed to improve the detecting precision [3]. Each pixel, in Qpix, possesses a SAR ADC allowing direct measurement of total charge. The GEM/Qpix experiment [4] demonstrates the ability of Qpix in 3D tracking applications. However, as a prototype chip, Qpix v.0 has no charge collection pad in each pixel and the data readout scheme is simple. Also, the power consumption of 350 μW/pixel should be reduced more.

Qpix v.1 has been developed to realize large area applications and to increase the basic performance. It possesses 400 pixels and compact readout structure to guarantee that all stored data in the pixels can be read out in 2.6 μs in parallel mode and 54 μs in serial mode. A charge collection pad is included in each pixel to realize large area applications. The SAR ADC in each pixel is optimized to 10 bit 10 MSps without area increase. Also, the offset calibration technology is applied to both the amplifier and the comparators to reduce the mismatch between pixels. The power consumption has been reduced to 187.5 μW/pixel.

2. Pixel Circuit

Fig. 1 shows a block diagram of the Qpix v.1 pixel cell. The pixel layout is shown in Fig. 2 (b). The active circuit measures 130 μm x 140 μm. The analog and digital circuits are designed to operate with separate 1.8 V power supplies. The basic idea of Qpix v.1 pixel cell is almost the same as Qpix v.0 pixel cell described in [3]. This paper focuses on the main upgrades in Qpix v.1 from Qpix v.0.

A pixel charge collection pad is integrated in each pixel and placed apart from the active circuits to avoid the crosstalk. The ESD devices for the pixel pad and decoupling capacitors for DC bias signals are placed under each pad to reduce the cell area. The pad size is designed to be as large as possible to back the possibility of coupling with the gas filled drift chambers, where the pixel pad will be used as an active anode to directly collect the charges generated in the gas chamber.

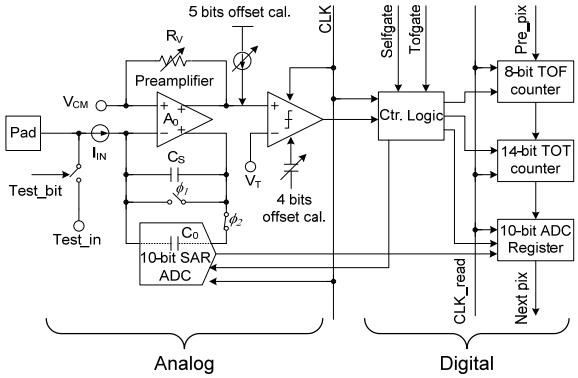

Fig. 1 Pixel structure

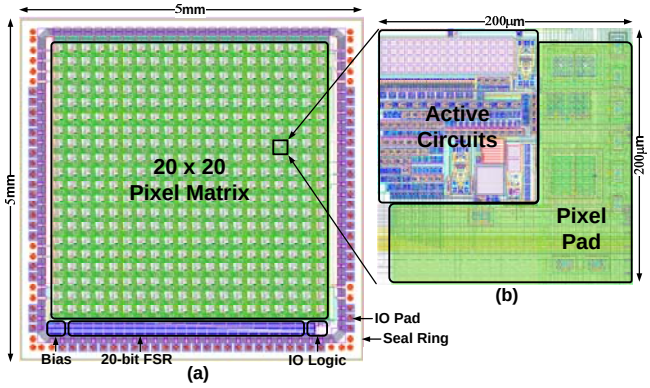

Fig. 2 Qpix v.1 chip: (a) chip layout and (b) pixel layout

A 5-bit current-steering DAC is implemented in the amplifier to reduce the offset voltage. The simulation result shows a 92% decrease of output offset voltage in all available I/V gain. The capacitive offset voltage calibration technique [5] is applied to the dynamic comparators. A 4-bit binary weighted capacitor array is used in each comparator. Simulation results show that offset voltage (σ) can be reduced from 13.5 mV to 1.5 mV. The decrease of output offset voltage in the amplifier and the input offset voltage in comparators can lower the detection threshold, and eventually increase the detection sensitivity.

The built-in pixel SAR ADC is optimized from 6 bits to 10 bits and kept conversion rate of 10 MSps without any increase of area. The charge measurement precision will be improved 16 times higher.

A linear feedback shift register counter works as a pseudo-random bit sequence counter during the acquisition period and works as a shift register during the data readout period. That is to say, there is no need for an additional circuit to shift the data out. In addition, a full custom de-

signed flip flop can reduce the cell size by about 37 % and the power consumption by about 40 % compared with that of the standard cell. All these efforts can reduce the die size and power consumption.

3. Chip Description

Qpix v.1 has been designed as convenient as possible for large detection area applications. Fig. 2 (a) shows the chip layout, with dimensions of 5 mm x 5 mm. The sensitive area is organized as a 20 x 20 pixels matrix and each pixel measures 200 μm x 200 μm. This results in a 16 mm^2 detection area (64 % of the total chip surface). Periphery circuitry includes DC bias circuits for pixel matrix, IO control logics, and a 20-bit fast shift register (FSR). The IO wire bonding pads are placed at the three sides of the chip. This arrangement is determined by considering the tradeoff between practicability, testability and realizability.

As mentioned in the last section, the charge collected in each pixel can be processed independently during the acquisition period. Counters will hold the time information and ADCs will represent the intensity of the corresponding particles. During the data readout period, the counters and the ADC register in each pixel, are arranged as a 32-bit shifter register as shown in Fig. 1. At the same time, this 32-bit shift register is connected to the neighboring shift registers in the same column. As a result, all the 32-bit shifter registers in the same column work as a 640-bit shift register. The data in the 20-column 640-bit shift registers can be shifted in parallel to the 20-bit FSR bit by bit. And finally, the data in the 20-bit FSR can be read out in parallel or in serial. The parallel readout mode is faster, while the serial readout mode is convenient for tiling Qpix v.1 chips together (for example, 2 x 2 chips) to get much larger detection areas. The highest readout rates both in parallel and serial are 500 Mbps. This high data readout rate is respected to demonstrate overwhelming advantages in any fast imaging hybrid systems [1].

As shown in Fig. 1, a test signal can be applied to Test_in port of each pixel in the matrix by setting the control bit: Test_bit. However, the total parasitic capacitance results in about 49 pF, since all the Test_in ports are connected together.

4. Measurements

Qpix v.1 was first tested by shifting out the initialized pixel registers data. Results show that IO logic circuits can work correctly up to 240 MHz (which is limited by our measurement environments) for both parallel readout mode and serial readout mode. This means that the measured data of the pixel matrix can be shifted out within 2.6 μs in parallel mode and 54 μs in serial mode.

Pixel function measurements were carried out using an external test pulse to input to the Test_in port of selected pixel. Typical measurement results shown in Fig. 3 indicate that Qpix v.1 can measure TOT and TOF with an accuracy of 10 ns, and the overflow function in TOT counter works correctly as designed. ADC codes show that the monotonicity can be kept however there is about 0.5 pC offset for the input range. The large parasitic capacitance in Test_in port is considered as the reason. More detailed measurements and GEM/Qpix experiments are in progress.

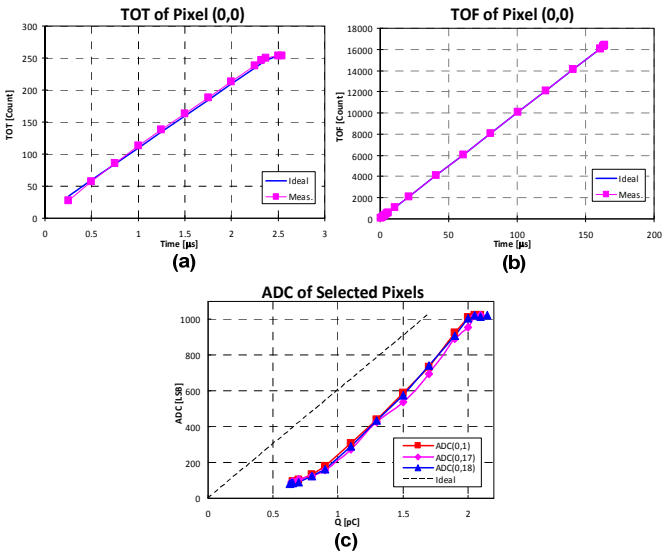

Fig.3 Measurement results: (a) TOT, (b) TOF, (c) ADC

The total power consumption is 75 mW (63 mW in the analog part and 12 mW in the digital part). Then the pixel power consumption is about 187.5 μW/pixel, which is about 54 % of the pixel power consumption in Qpix v.0.

5. Conclusions

The Qpix v.1 prototype chip integrating charge collection pad in each pixel and 400 pixel cells of 200 x 200 $μm^2$, has been developed using 0.18 μm CMOS commercial process to realize large area applications for particle detectors and to increase the basic performance. The stored data in the pixels can be read out in a short time of 2.6 μs in parallel mode and 54 μs in serial mode. The pixel SAR ADC is optimized to 10 bit 10 MSps without area increase. Also, the offset calibration technology is applied to reduce the mismatch between pixels. The power consumption of total chip and each pixel were measured as 75 mW and 187.5 μW, respectively. The preliminary measurements validated all functions of the pixel.

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