A 0.5V 1.4mW 750MHz 10b CMOS Current Steering DAC

Naoki Shimasaki, Robert Ito, Masaya Miyahara, and Akira Matsuzawa

Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27, Ookayama, Meguro-Ku, Tokyo 152-8552, Japan. Phone/Fax: +81-3-5734-3764

1.   Abstract

An ultra-low voltage operation of 0.5 V and an ultra-low power consumption of 1.4 mW that is at least one order magnitude lower than that ever reported, yet high speed of 750 MHz CMOS 10 bit current staring DAC has been developed. Careful low voltage circuit design for the bias circuits with digitally assisted technique instead of the conventional feedback circuit using operational amplifier and a forward body bias technique that can increase operating frequency twice under the ultra-low voltage operation of 0.5 V have been introduced to address the ultra-low voltage analog circuit design issues.

2.   Introduction

An ultra-low voltage operation such as 0.5 V in mixed signal SoC becomes important circuit design technique to reduce the power consumption for realizing real green portable electronics and to address future technology scaling where the operating voltage will be reduced and current mixed signal CMOS circuit techniques will loose the validity.

A high speed current steering Digital to Analog Converter (DAC) is an important interface circuit to generate many kind of analog signal waveforms such as for wireless or wireline communications, HDD, DVD, and digital TV applications. It is however quite difficult to design 0.5 V DAC with high accuracy of 10 bit due to need of stacking transistors to realize sufficient accuracy of output current. Furthermore the use of an operational amplifier to stabilize the current is impossible under the ultra low voltage operation. Also high conversion frequency of about 1 GHz is another issue because the gate delay increases drastically with operating voltage lowering down to 0.5 V.

To address these issues, we have developed low voltage circuit design for the bias circuits using digitally assisted technique with dynamic latch instead of a conventional operational amplifier and forward body bias technique.

3.   Ultra-Low voltage circuit design

a) A unit current cell

We used a simple PMOS unit current cell shown in figure 1. A cascode circuit booting output impedance is required to realize sufficiently small INL for 10 bit resolution; however it is very difficult to stack the transistors to realize the cascode circuit with switching transistor. Therefore, we used switching transistors M_{p2r} and M_{p2L} as a cascode transistor by selecting the threshold voltage and adjusting the effective gate voltage V_{eff} (V_{gs}-V_T) to satisfy the saturation condition for each transistor. The single output voltage of 0.2 V, the differential output swing of 0.4 V, the unit current of 2 μA, the total current of 2 mA, and the

output impedance of 6 MΩ   are estimated.

b) Digitally controlled bias circuit

Output current should be stabilized to the PVT fluctuations and a feedback circuit with an operational amplifier (OpAmp) is used conventionally. However it is difficult to use high gain OpAmp with 0.5 V power supply. Therefore we used digital control circuit as shown in figure 2, instead of a conventional OpAmp. A dynamic comparator compares reference voltage, V_{ref} and an appeared voltage on R_{ref}. The counter integrates the number of pulses from the comparator and 8 bit resistor ladder DAC generates the bias voltage V_B according to the counter output. The bias voltage can settle within 256 clocks. Figure 3 shows the current stability against the fluctuation of power supply voltage and temperature. Less than 1 % errors will be realized over estimated fluctuations.

c) Logic gates with forward body bias

Gate delay time will increase and operating frequency will decrease so much when the supply voltage is reduced to 0.5 V. The forward body bias technique is used to address this issue. At the ultra low voltage less than the built-in potential of PN junction, the forward body bias operation can be realized easily to connect the body of NMOS to V_{DD} and the body of PMOS to the ground. This configuration makes circuit and layout simple, as shown in figure 4(a). The gate delay time can be reduced about half for the conventional CMOS circuit, as shown in figure 4(b).

4.   Measurement result

An ultra-low voltage CMOS DAC has been fabricated in 90 nm CMOS process with a deep-Nwell option. Figure 5 shows a chip layout. The occupied area is 0.092 mm^2.

Figure 6 shows a measured nonlinearity at the conversion frequency of 750 MHz. The INL is less than 1.7 LSB and the DNL is less than 0.9 LSB.

Figure 7 shows the Spur Free Dynamic Range (SFDR) vs. the input frequency and the conversion frequency. The SFDR of over 56 dB has been measured until the conversion frequency of 750 MHz at the input frequency of 10 MHz.

The SFDR of 56 dB has been obtained for the input frequency of 10 MHz at the conversion frequency of 750 MHz.

The power consumption excluding the output current is only 1.4 mW (Analog: 0.75 mW and Digital: 0.65 mW) at 0.5 V and 750 MHz operation. Table 1 summarizes the measured performance and compares the previous works [1] [2]. The power consumption can be reduced dramatically.

5. Conclusions

A careful low voltage circuit design for the bias circuits with digitally assisted technique instead of the conventional feedback circuit using operational amplifier and a forward body bias technique that can increase operating frequency twice under the ultra low voltage operation of 0.5 V have been introduced to realize an ultrla-low voltage DAC. As a result, A 0.5 V, 1.4 mW that is at least one order magnitude lower than that ever reported, 750 MHz, 10 b CMOS current Steering DAC has been realized.

References

[1] Chueh-Hao Yu, et al., "A 90nm 10-bit 1GS/s current-steering DAC with 1-V supply voltage," IEEE International Symposium on VLSI Design, pp.255-258, April 2008.

[2] Kuo-Hsing Cheng, et al., "A 1-V 10-bit 2GSample/s D/A converter based on precision current reference in 90-nm CMOS," IEEE International Conference on Electronics, Circuits and Systems, pp.340-343, September 2008.
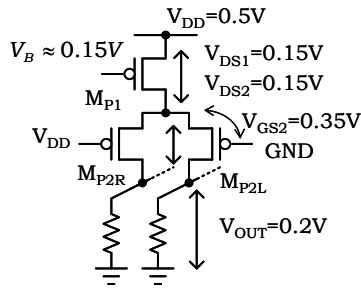
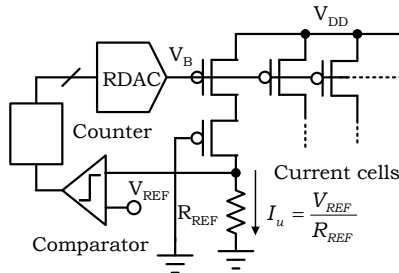Fig. 1. A unit current cell circuit and bias voltages.

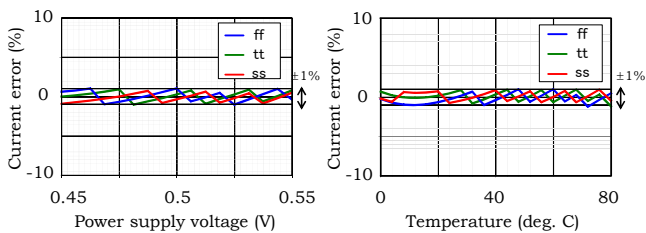
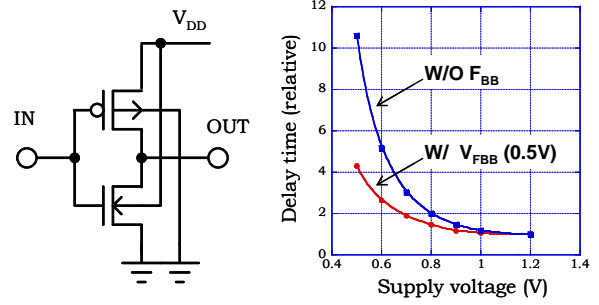Fig. 2. Digitally controlled bias circuit without OpAmp.

Fig. 3. Current stability against the fluctuation of power supply voltage and temperature.

(a) Logic gates with FBB   (b) Gate delay time vs. V_{DD}

Fig. 4. Logic gates with forward body bias (FBB) and the gate delay time vs. supply voltage.
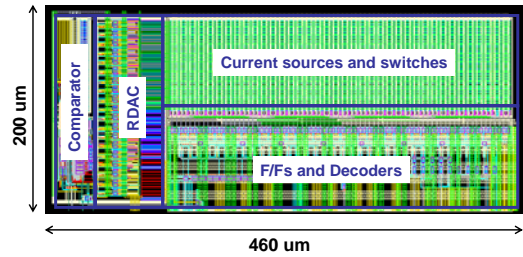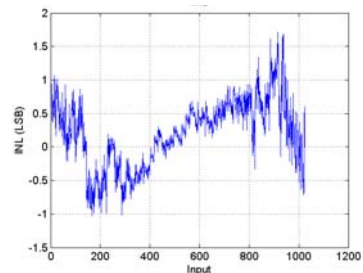

Fig. 5. Chip layout.
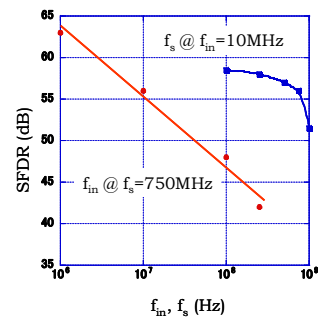

Fig. 6. Non-linearity (INL).

Fig. 7. SFDR vs. f_{in} and f_s.

Table 1. Performance summary and comparison.

Reference	VDD (V)	fc (GHz)	Io (mA)	Pd (mW)	INL (LSB)	DNL (LSB)	SFDR (dB)
[1]	1.0	1.00	13	13.0	N/A	N/A	64.8 @50MHz
[2]	1.0	2.00	8	71.0	0.14	0.4	71.2 @10MHz
This work	0.5	0.75	2	1.4	1.7	0.9	56.0 @10MHz