Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1166-1167

G-7-4L

3.6-Times Higher Acceptable Raw Bit Error Rate, 97% Lower-Power, NV-RAM & NAND-Integrated Solid-State Drives (SSDs) with Adaptive Codeword ECC

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1. Introduction

This paper proposes the adaptive codeword ECC (Error Correcting Code) for NV-RAM (Non Volatile RAM) and NAND flash memory integrated SSD to improve the memory cell reliability by 3.6-times. In the proposed SSD, NV-RAM such as RRAM, PRAM and MRAM is used as write buffers (Fig.1 and Table 1). 16 NAND channels operate at the same time while single NV-RAM chip operates. The NV-RAM write buffer compensates the 10-100 times performance gap [1] between the NAND flash memory and the SSD interface (Fig.2) and realizes the 10Gbps write. During the write, data are first stored in NV-RAM at 10Gbps. Then, data in NV-RAM are transferred to NAND with a sustained write speed of 2.6Gbps (Fig.1(b)). During the read, data output from NAND to the controller by bypassing NV-RAM (Fig.1(c)). At 10Gbps, the proposed SSD decreases the power consumption by 97%. DRAM is not suitable for write buffers since data in DRAM are lost in case of the power outage. In the proposed ECC, errors of both NV-RAM and NAND are corrected without circuit area overhead by sharing ECC circuits. The ECC codeword, the data unit where ECC is performed, is adaptively optimized for NV-RAM and NAND. The ECC codeword is 32KByte for NV-RAM and 2KByte for NAND. The acceptable raw bit error rate before ECC increases by 3.6-times without ECC circuit area/power consumption penalty.

2. Power Consumption Comparison

In the conventional SSD, the write speed is enhanced by increasing the number of channels (N_{NAND}), that is, the number of NAND chips written/read in parallel (Fig.3) [2]. A high-speed NAND interface, 16IOs with 40MHz DDR is assumed. The write speed of the conventional SSD is determined by the memory cell write and is not accelerated by increasing IOs. In contrast, in the proposed SSD, the write speed is enhanced by increasing the number of IOs of the single NV-RAM (N_{IO}) (Fig.4). Fig.5 compares the SSD power consumption, P_{SSD}. In the conventional SSD, $P_{SSD\_Conventional} = N_{NAND}$ x 50mA x 3V. Single NAND chip consumes 50mA with 3V power supply. In the proposed SSD, $P_{SSD\_Proposed} = N_{IO}$ x 29mA x 1.5V where 1.6GHz DDR3 interface without a refresh is assumed. At 10Gbps, in the conventional SSD, N_{NAND} is as many as 68 because the single NAND speed is as low as 0.16Gbps. In contrast, in the proposed SSD, N_{IO} is only 7. As a result, $P_{SSD\_Conventional}$ and $P_{SSD\_Proposed}$ are 10.2W and 0.3W. The power consumption of the proposed SSD decreases by 97%.

3. Integrated ECC for NV-RAM and NAND

Single ECC Scheme

This paper proposes the integrated ECC for NV-RAM and NAND which corrects errors of both NV-RAM and NAND. In the high density NV-RAM such as MRAM [3] and PRAM [4] memory cell errors are inevitable and ECC is required. The proposed ECC is implemented in the NV-RAM/NAND controller (Fig.1). This paper compares three ECC schemes (Fig.6-8 and Table 2). In the single ECC (Fig.6), the error correction is performed only once with 2KByte codeword. The ECC encoding, that is, the parity generation operates before data is written to NV-RAM. In the ECC decoding, errors are corrected for data output from NAND. ECC is required for each memory channel [5]. For 16 NAND channels, 16 ECC circuits are required.

Proposed Shared ECC Scheme

In the proposed shared ECC (Fig.7), ECC is performed twice for NV-RAM and NAND. The 1st ECC encoding is performed before data input to NV-RAM. When data in NV-RAM are transferred to NAND, errors of NV-RAM are corrected in the 1st ECC decoding. The 2nd ECC encoding is performed before data are written to NAND. As data output from NAND, errors of NAND are corrected in the 2nd ECC decoding. Because errors of NV-RAM and NAND are corrected independently, twice as many errors are allowed compared with the single ECC. The 1st and the 2nd ECC encoding may operate simultaneously if the input data are more than the capacity of NV-RAM. Thus, two separate ECC encoders are required. On the other hand, the 1st and the 2nd ECC decoding do not happen at the same time because the SSD read and write do not occur simultaneously. Thus, the ECC decoder is shared. The circuit area of the ECC encoder is less than one-tenth of the ECC decoder [5]. In the shared ECC, even if ECC encoders doubles compared with the single ECC, the circuit area of the overall ECC, encoders and decoders, increases less than 1%.

Proposed Adaptive Codeword ECC Scheme

This paper also proposes the adaptive codeword ECC (Fig.8). Similarly to the shared ECC, the error correction is performed twice for NV-RAM and NAND. The ECC codeword of NV-RAM is larger than that of NAND to achieve a higher reliability. As the ECC codeword is larger, the acceptable raw bit error rate before ECC is larger (Fig.9). As a drawback, the circuit area and the power consumption of the ECC decoder increase. Thus, the ECC codeword is maximized to enhance the reliability under the constraint of the circuit area and the power consumption [5].

For the ECC of NAND, because 16 NAND channels operate to achieve a 10Gbps read, 16 ECC circuits are required. The codeword of NAND is 2KByte. On the other hand, in the ECC of NV-RAM, only one NV-RAM chip operates because the required speed is 2.6Gbps which is restricted by the 16 channel NAND write (Fig.8). For the ECC of NV-RAM, only one ECC circuit is required and thus 16-times as much circuit area and power consumption are allowed compared with the ECC of NAND (Fig.10). The codeword of NV-RAM is extended to 32KByte. As a result, the acceptable raw bit error rate before ECC of NV-RAM increases by 2.6-times (Fig.9). The total acceptable raw bit error rate before ECC of NAND and NV-RAM increases by 3.6- and 1.8-times compared with the single ECC and the shared ECC, respectively. The ECC circuit area overhead is negligibly small because the same ECC decoder is used for NV-RAM and NAND.

4. Conclusions

An adaptive codeword ECC is proposed for the NV-RAM and NAND integrated SSD. Errors of NV-RAM and NAND are most efficiently corrected and the reliability improves by 3.6-times without circuit area overhead. By using NV-RAM as write buffers, the 10Gbps write is achieved with a 97% power reduction.

Acknowledgements

The authors appreciate A. Esumi, M. Ito and K. Li for their support.

References

[1] K. Takeuchi, *International Memory Workshop*, pp. 13-16, 2010. [2] K. Takeuchi, *Symp. VLSI Circuits*, pp. 124-125, 2008. [3] R. Nebashi, et al., *ISSCC*, pp.462-463, 2009. [4] Y.N.Hwang, et al., *Symp. VLSI Technology*, pp. 201-202, 2010. [5] S. Tanakamaru, et al., *International Memory Workshop*, pp. 88-91, 2010.

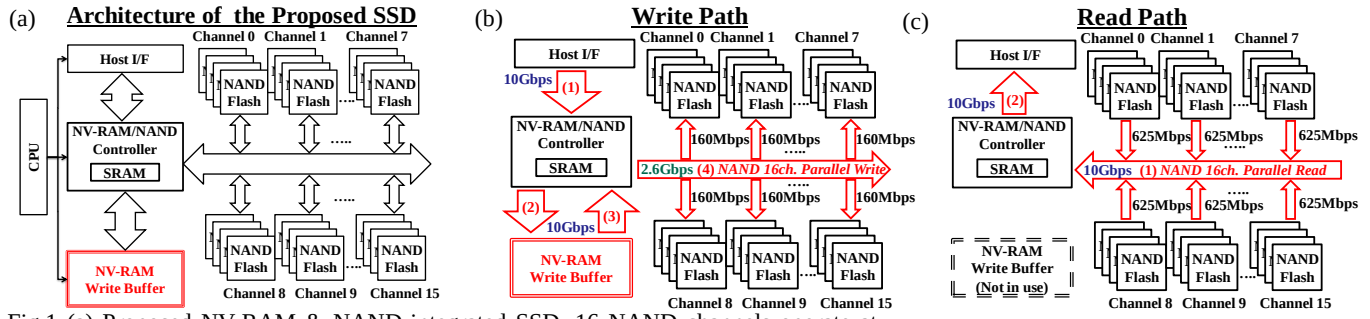


Fig.1 (a) Proposed NV-RAM & NAND-integrated SSD. 16 NAND channels operate at the same time while single NV-RAM chip operates. (b) Write operation. First, the write data is stored in NV-RAM at 10Gbps. Then, data are transferred to NAND at 2.6Gbps. (c) Read operation. Data are directly read from NAND to the controller at 10Gbps.

Table 1 Characteristics of the proposed SSD.

	Read	Buffered Write	Sustained Write
Speed	10Gbps	10Gbps	2.6Gbps

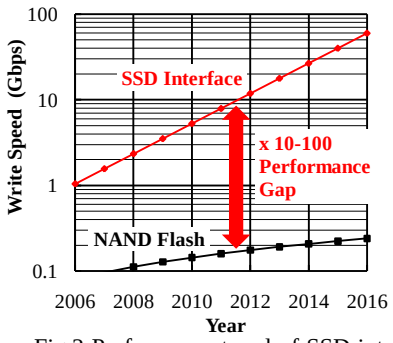


Fig.2 Performance trend of SSD interface and NAND flash memory [1].

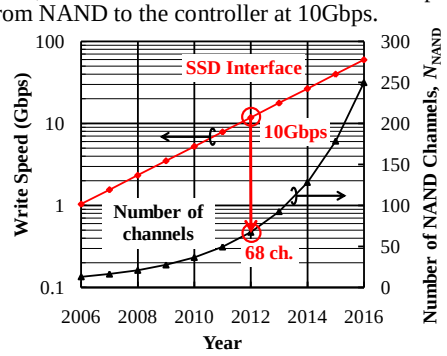


Fig.3 Trend of number of NAND channels. As many as 68 NAND channels operate to write NAND chips at 10Gbps.

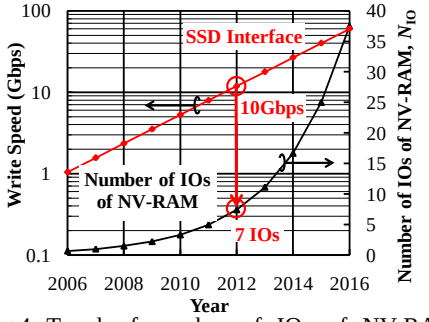


Fig.4 Trend of number of IOs of NV-RAM. DDR3 interface with 1.6GHz is assumed. Only 7 IOs are required to write NV-RAM at 10Gbps.

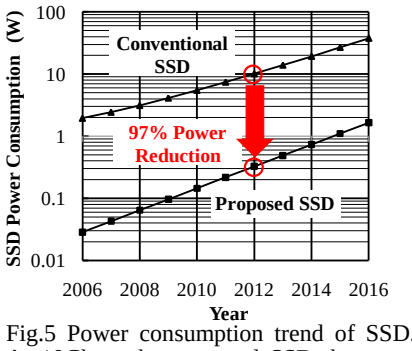


Fig.5 Power consumption trend of SSD. At 10Gbps, the proposed SSD decreases the power consumption by 97%.

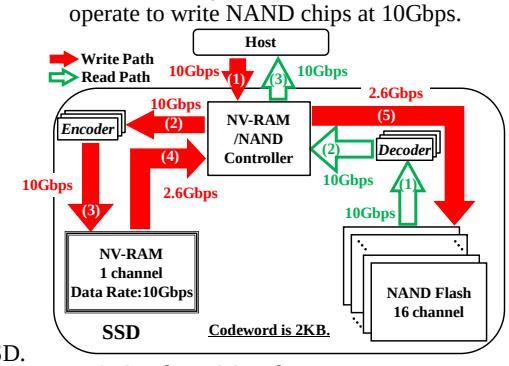


Fig.6 Single ECC. The error correction is performed only once with 2KByte codeword.

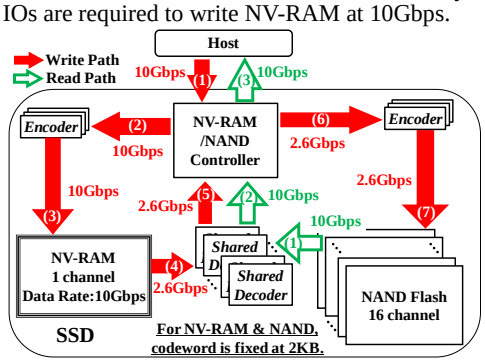


Fig.7 Proposed shared ECC. ECC is performed twice for NV-RAM and NAND, respectively with 2KByte codeword.

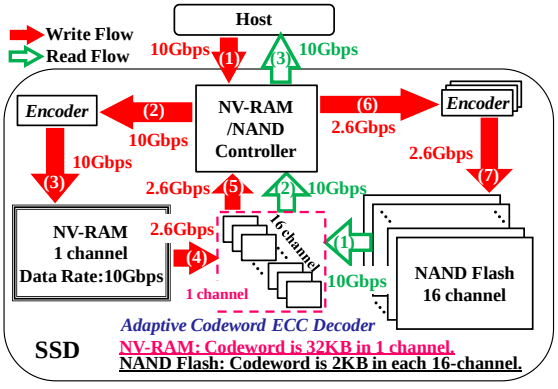
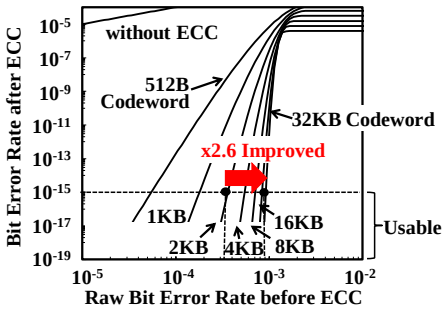


Fig.8 Proposed adaptive codeword ECC. The ECC codeword for NV-RAM and NAND is 32KByte and 2KByte, respectively.

Table 2 Comparison of single ECC, proposed shared ECC and proposed adaptive codeword ECC.

	Single ECC	Proposed Shared ECC	Proposed Adaptive Codeword ECC
Acceptable Raw Bit Error Rate (NAND)	3.6×10^{-4}	3.6×10^{-4}	3.6×10^{-4}
Acceptable Raw Bit Error Rate (NV-RAM)		3.6×10^{-4}	9.2×10^{-4}
Acceptable Raw Bit Error Rate (Total: NV-RAM&NAND)	3.6×10^{-4} (x 1)	7.2×10^{-4} (x 2)	12.8×10^{-4} (x 3.6) (x 1.8)
ECC Codeword (NAND) [channel number]	2KByte [16ch]	2KByte [16ch]	2KByte [16ch]
ECC Codeword (NV-RAM) [channel number]		2KByte [16ch]	32KByte [1ch]
ECC circuit area (mm^2)	12.9 (x 1)	13.0 (x 1.01)	13.0 (x 1.01)



ECC codeword	2KByte	4KByte	8KByte	16KByte	32KByte
Acceptable raw bit error rate before ECC	3.6×10^{-4} (x 1)	5.5×10^{-4} (x 1.5)	7.1×10^{-4} (x 2.0)	8.4×10^{-4} (x 2.3)	9.2×10^{-4} (x 2.6)

Fig.9 Bit error rate after ECC vs. acceptable raw bit error rate before ECC. In the proposed adaptive codeword ECC, the acceptable raw bit error rate before ECC of NV-RAM increases by 2.6 times by increasing the codeword from 2K to 32KByte.

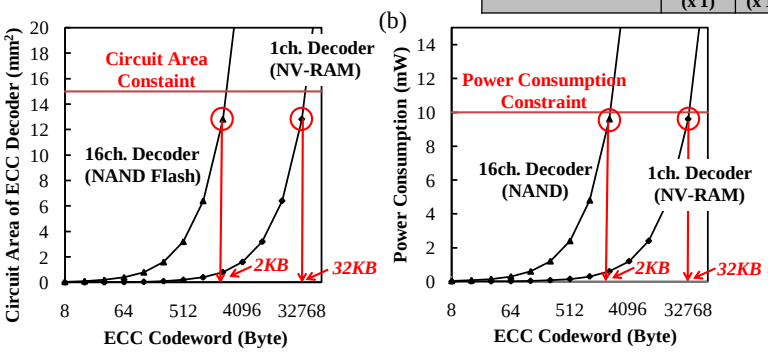


Fig.10 (a) Circuit area of ECC decoders vs. ECC codeword. (b) Power consumption of the ECC decoders vs. ECC codeword. As the ECC codeword is larger, both the circuit area and the power consumption of the ECC decoder increase. In the single ECC or the shared ECC, the optimal codeword is 2KByte. In the adaptive codeword ECC, the optimal codeword is 32KByte.