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Fabrication of CMOS-compatible Poly-Si Nanowire FET Sensor

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1. Introduction

Silicon nanowire field effect transistors (Si NW FET) are emerging as electrochemical sensors for biological and chemical species detection [1][2]. Recent research shows Poly-Si nanowires FET (PSNW) act as a high sensitivity biosensors with even more simplified process and cost reduction [3]. In this work, we demonstrate a low-cost, superior uniformity, and stable PSNW FET sensor fabrication method that features entire CMOS processing. A two-step trimming approach based on I-line lithography scales down the NW channel dimension to 35 nm. The real-time and reversible pH sensing functionality indicates PSNW FET is attractive for potential electrochemical sensing applications. In addition, a unique method to fabricate the self-aligned PSNW FET and CMOSFET simultaneously in the production bulk-Si technology is disclosed for the first time. This work demonstrates a simple electrochemical sensor fabrication with a fully CMOS-compatible process. This integration method is crucial for cost-efficient, compact, and high performance sensor system demonstration.

2. Low-cost Poly-Si nanowires fabrication

Figure 1 shows the process flow of the buried channel Poly-Si nanowires (PSNW) FET. After the I-line lithography, the wafer underwent photoresistor trimming and then plasma etching to form the slender channel. To further trim the PSNW dimension, a 900 °C, 1.5-hour thermal oxidation process with a oxide removal process was used. Figure 2 shows the SEM and TEM picture of the PSNW channel. After oxidation trimming, the line edge roughness of PSNW is preserved and the channel surface to volume ratio is approximate 70% increased for PSNW sensitivity enhancement. Figure 3 shows the PSNW schematic and the FET I_d-V_g characteristic. Figure 4 shows this buried channel PSNW FET saturation current within wafer distribution with 32-die measurement. The PSNW exhibits tighter current distribution and superior performance after the thermal oxidation process which suggests possible grain boundary trap elimination. The tighter distributions mean a higher production yield and more accurate detection ability for nanosensor. Subsequently, a plasma treatment is employed after S/D activation. The NH_3 plasma treatment lasts 30 minutes which passiavtes the dangling bond of the PSNW buried channel interface [4]. This unique process improves the device stability in the aqueous solution environment.

3. Poly-Si NW pH sensing functionality

Figure 6 shows the real-time device I-V measurement. The device shows subthreshold-swing and performance improvement when it operates in aqueous solution due to the poly grain boundary trap passivation effect [5]. The devices threshold voltage shift to the more negative when the pH of solution changes from 5 to 9 and recovers to near the original level when the pH value goes back to 5. The protonation or deprotonation reactions occurs at the native oxide surface of the devices when the solution pH value is altered. The electrochemical reactions generate positive or negative charges due to charging and discharging of the interface state at Poly-Si channel surface which modify the buried channel electric field and lead to devices threshold voltage shift. The result shows that the PSNW device is sensitive and repeatable to response in surface charge variations that are preferable for electrochemical detection.

4. Self-aligned trench Poly-Si NW fabrication in CMOS

We disclose a unique method to fabricate the self-aligned trench PSNW and conventional CMOSFET simultaneously in a single substrate using a completely manufacturing CMOS process. Figure 7 shows the process flow. The PSNW forms through an extra STI oxide recess induced Poly spacer formation around the strip Si after Poly gate patterning. Figure 8 shows the TEM cross-sectional view of this PSNW and its bulk-Si gate electrode. Part of the nanowire channel is exposed to the environment hence this exposed surface could serve as the sensing site for electrochemical reactions. This PSNW formation is self-aligned and can be integrated in the mature CMOS process for superior uniformity control, highly integrated system design and involves no costly lithography tool. Figure 9 shows and investigates the TCAD simulation for elementary FET characteristics and channel carrier responses to surface charge. This demonstration is the first to create the PSNW FET in the standard CMOS front-end process without costly and complex process integration in a bulk-Si substrate.

5. Conclusion

In this work, we demonstrate the low-cost and high production yield Poly-Si nanowire FET devices fabrication for electrochemical sensor application. The device uniformity is well controlled using manufacturing process and the highly integrated process will serve as the interface to connect the sensor and logic devices. It discloses a new way for future portable and low cost sensor system on a chip for healthcare application using mass production semiconductor technology.

Acknowledgement

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References

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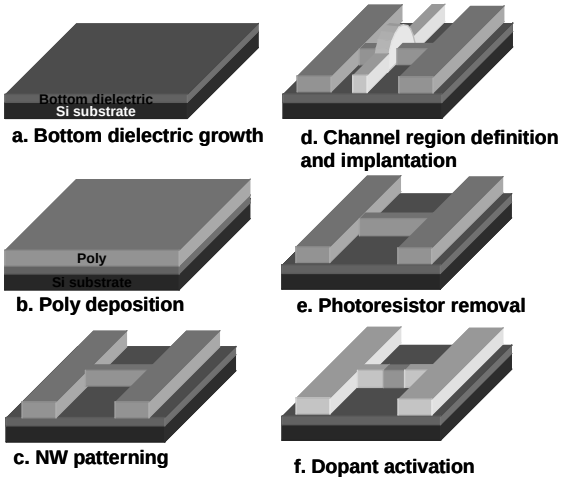

Fig.1 The Poly-Si nanowire FET fabrication process flow. A 10 keV and 5×10^{15} /cm^2 Phosphorus implantation is used for S/D pad resistance reduction. A 900 ˚C, 30 sec RTA is performed for dopant activation

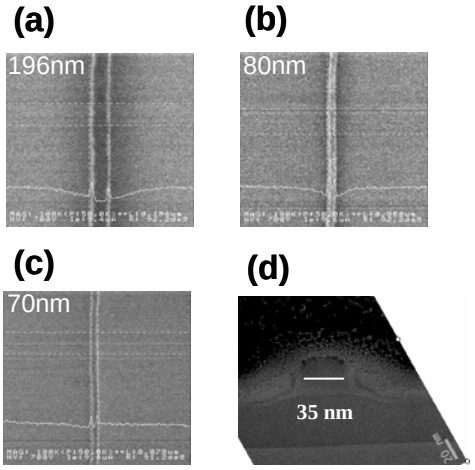

Fig.2 The top-down SEM images of the Poly-Si nanowire two-step trimming process flow. (a) The nanowire photoresistor pattern after I-line exposure. (b) The photoresistor pattern after first plasma trimming. (c) The nanowire after Si etch and thermal oxidation trimming. (d) The cross-sectional TEM image of two-step trimmed nanowire.

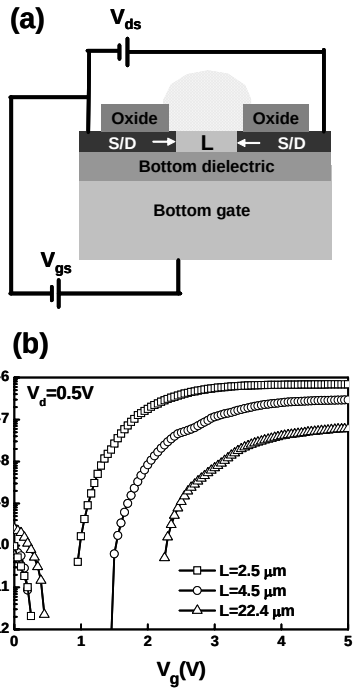

Fig.3 (a) The schematic illustration of nanowire FET electrically testing configuration. (b) The Poly-Si nanowire FET I_d-V_g characteristics with various channel length.

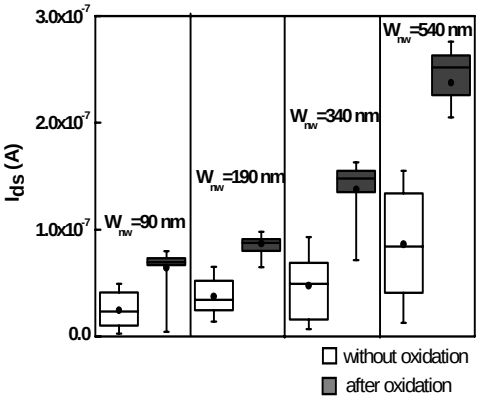

Fig.4 The within wafer PSNW FET I_{dsat} distribution with various nanowire width measured by SEM before oxidation. Those devices with second oxidation trimming show superior current uniformity and device performance.

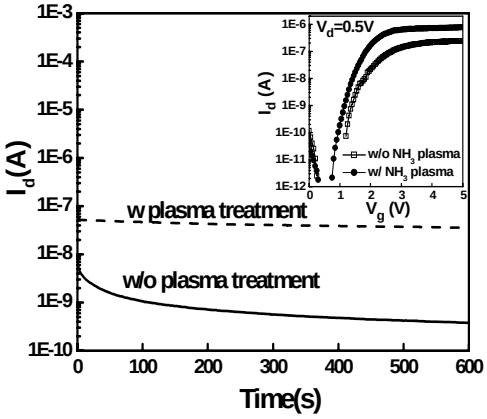

Fig.5 The NH_3 plasma treatment improves the Poly-Si nanowire FET performance and stability under high V_g (V_g=5V) stress condition in the aqueous

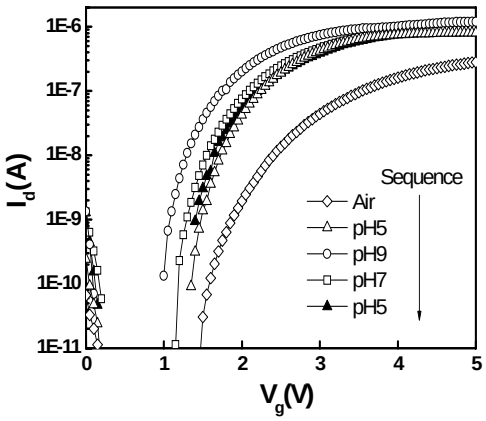

Fig.6 The real-time Poly-Si nanowire FET I_d-V_g measurement in aqueous solutions with varied pH concentration. The testing sequence is showed by the arrow symbol. Each testing is performed after the solution is injected to the channel for 5 min.

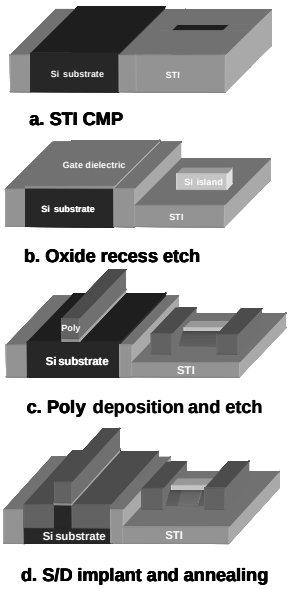

Fig.7 The self-aligned trench Poly-Si nanowire FET fabrication process flow.

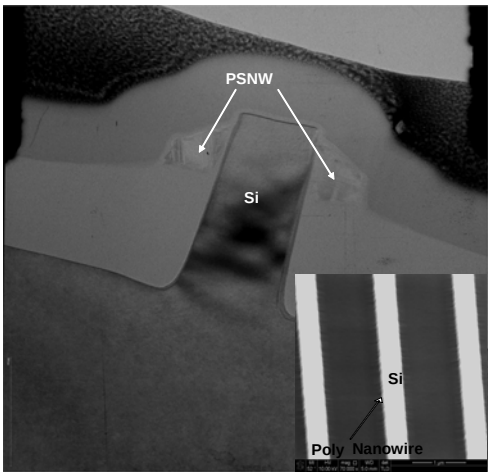

Fig.8 The cross-sectional TEM image of self-aligned trench Poly-Si nanowire FET. Inset shows the tile-angle view of trench spacer Poly-Si nanowire array.

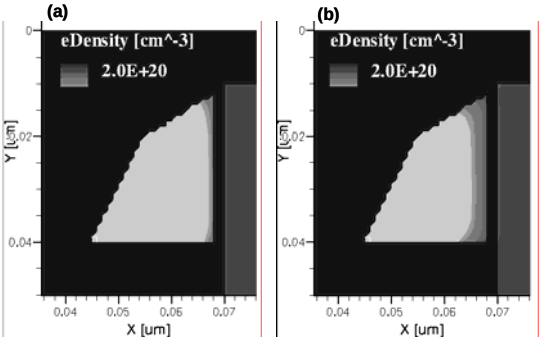

Fig.9 The TCAD simulation of self-aligned trench Poly-Si nanowire FET electron density contour at V_g=0.1 V. (a) No charge at the device surface. (b) The positive fixed charge at the device surface with density up to 1×10^{10}/cm^2. The gray region indicates the electron density contour which set the 1×10^{18}/cm^3 as start-up concentration.