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Improvement of Variability and Reliability in Low-k/Cu Interconnects by Selectivity Control in Dry-Etching Process

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1. Introduction

In the scaling of LSI technology, precise control of the patterning profile in low-k films has become a critical issue to keep high reliability and small variability in Cu dual damascene (DD) interconnects. Chemical composition of C/Si ratio in the low-k SiOCH films and etching gas affect the selectivity in the reactive ion etching (RIE) to open via and trench patterns in the via-first (VF) DD process, which directly impacts on the reliability and variability (Fig.1). Highly-selective low-k etching against the SiCN-cap at the via-bottom is required to prevent oxidation of the underlying Cu during the following ashing step. High etching selectivity of the hard mask (HM) against the low-k suppresses the variation of the trench depth.

In this work, we investigate effects of RIE process, along with the chemical composition of the low-k dielectrics, on the variability and reliability of Cu DD interconnects.

2. Experimental

Double-layered Cu interconnects were fabricated through the VF-DD process (Fig.1). Two types of low-k SiOCH films with high carbon content (high-C) or low carbon one (low-C) were investigated with SiO_2-HM and SiCN-cap layers (Table.1). Here, the high-C film with C/Si=2.7 was MPS (Molecular-Pore-Stack) SiOCH film with k=2.55[(1], while the low-C film with C/Si=0.6 was a rigid SiOCH with k=3.0. The low-k films were sandwiched between the SiO_2-HM (C/Si=0) and SiCN-cap (C/Si=0.9) in the patterning process. Electrical properties of the sheet resistance (Rs) and interconnect capacitance were measured for the upper-level interconnects to evaluate the variability. The via yield and the reliability, such as stress-induced-voiding (SiV) and electro-migration (EM), were evaluated for 66 nm-diameter vias.

3. Results and Discussion

(a) Variability in Cu Lines:

The resistance variability of Cu lines is affected by variation in the trench depth, which has been caused essentially by micro (μ)-loading effects and plasma non-uniformity across a wafer. To reduce variability in the line resistance, it is a key to suppress the over-etching depths for various line-widths in the low-k film during the HM-etching step. The variation in the over-etching depth into the low-k film enhances the trench-depth (D) fluctuation by the following low-k etching step.

In case of the low-C SiOCH film, however, it was hard to limit the over-etching depth due to a lack of selectivity in the HM etching with a fluorocarbon-based etching gas, and the pattern-size effect on Rs increased (Fig.2). The variations of Rs in a 300 mm wafer also were greater than $\pm$10% ($\pm 3\sigma$) for the line widths from 66 to 462 nm (Fig. 3). As for the high-C film, carbon-based polymers were deposited in the over-etching step due to a plenty of C in the film, acting as an etching stopper. High selectivity to the low-k etch minimized the variability of trench depth, resulting in constant Rs of the Cu lines wider than 0.2 μm (Fig.2). The variations in Rs were suppressed below 10% in the Cu lines, irrespective of the line width. (Fig.3)

Fig. 4 shows interconnect RC plots of the 132 nm-pitch Cu-lines. It is noted that, the variations of RC, especially of the Rs, with the high-C film were much smaller than those with the low-C. For narrow lines below 100 nm-width, Rs increases abruptly by electron scattering effect, and small change in the cross-sectional area, or essentially the trench depth (ΔRs/ΔD) of the narrow Cu lines, enlarge the Rs variability. Namely, the high-C MPS interconnect with excellent controllability of the trench-depth has not only the lower interconnect parasitic capacitance, but also the smaller RC variability.

(b) Yield and Reliability of Cu-vias:

For the via patterning in the high-C MPS film, addition of N_2 into the fluorocarbon-based gas chemistry removed the carbon-based polymers on the etching surface to enhance the etching rate even with a small amount of fluorocarbon gas[(2,3]. (Fig. 5) Reduction in fluorocarbon gas decreased the etching rate of the Si-rich SiCN (Fig.5) at the via bottom during the over-etch step. Thus, high selectivity, approximately 10, was achieved by optimization of N_2 and fluorocarbon in the gas chemistry.

The SiCN thickness remained at the via bottom, which had been determined by the etching selectivity and the over-etch time, was critical for the via yield (Fig. 6(a)). Since the SiCN film was found to be oxidized up to 10nm during the ashing step in the via-etch sequence (Fig. 6(b)), the oxygen would reach the Cu surface under the via through thin SiCN to decrease the via yield. Electron energy-loss near-edge structures (ELNES) of the Cu L-edge confirmed that the Cu under the via was oxidized when the SiCN thickness was less than 10 nm after the via etch (Fig. 7).

Under the SiV test (175 ^{o}C, 168 H), the via resistance was stable for the samples with the remained-SiCN thickness greater than 10 nm (Fig.8). The EM lifetime was also improved by increasing the remained SiCN thickness over 10 nm, probably due to suppression of the Cu oxidation at the via bottom (Fig. 9).

4. Conclusions

The carbon-rich MPS film achieved highly selective RIE processes, accomplishing small variability and high reliability. The precise control of the selectivity both in the trench and via etching sequences is a key to reduce the variability in Rs and the via reliability in Cu DDIs.

References: 1) M. Ueki, et al, IEDM2008 pp. 619-622 (2008). 2) M. Fukasawa, et al, J.Vac.Sci. Techol.A.(2008), 3) M.Hori. ECS Trans. 2007, pp.485-500 (2007).

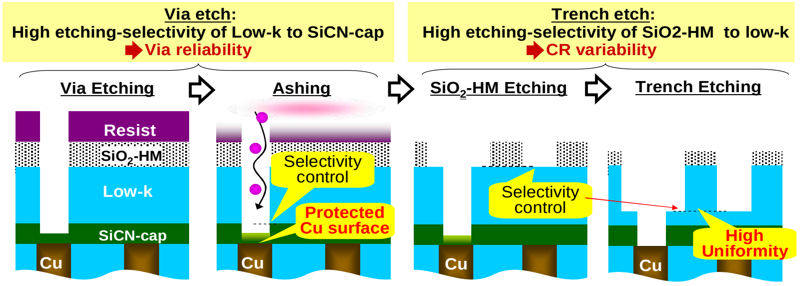

Fig.1 Process flow of the via first (VF) dual damascene (DD) patterning and key points for high reliability and low variability in the Cu/low-k interconnects.

Table.1 Film composition (C/Si ratio) and critical factors for high selectivity in the DD patterning.

	C/Si	Factors for high selectivity
HM (SiO_2)	0	**HM/Low-k interface:** Deposition of carbon-based polymer as an etch-stopper.
Low-k	Low-C: 0.6 High-C: 2.7	**Low-k/Cap interface:**
Cap (SiCN)	0.9	-Polymer removal by N_2 in etching gas. -Low rate of Si-rich cap.

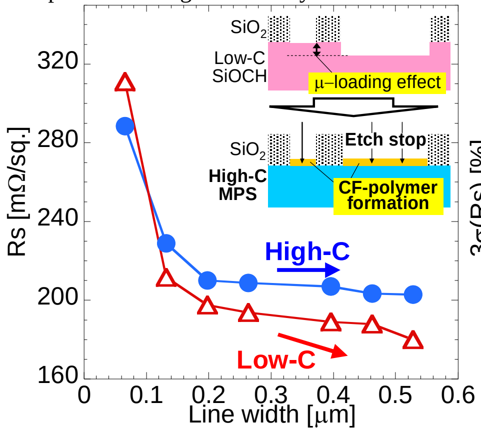

Fig.2 The sheet resistance Rs as a function of line width. High Rs at narrow line is attributed to the pattern-size effect on metal resistivity. Continuous decrease in Rs at the wide width for the Low-C is due to µ-loading effect at the HM/low-k interface.

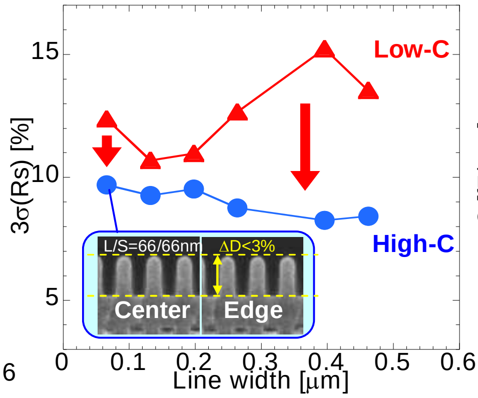

Fig.3 The variability (±3σ) of Rs with different low-k structures. Variability in Rs for the Cu lines with high-C film is much lower than that with low-C film, due to high selectivity of HM to the low-k film.

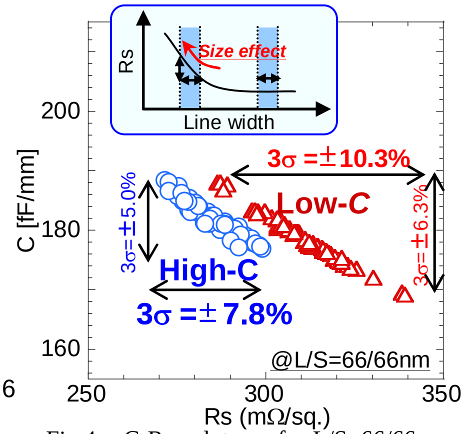

Fig.4 C-R plots of L/S=66/66nm interconnects with the high-C and low-C structures. Slight increase in capacitance variation for the low-C, due to profile variation, causes significant variability in Rs, suffered from the pattern-size effect of electron scattering in fine metal lines.

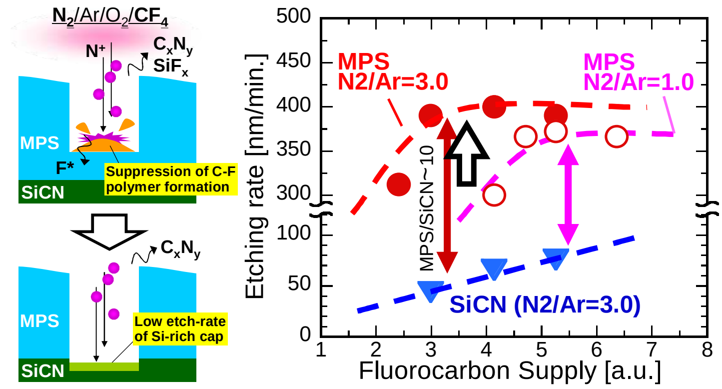

Fig.5 Enhancement of MPS/SiCN selectivity at the via bottom in the via patterning step. Nitrogen suppresses the polymer deposition during the MPS (high-C) etching to keep a high etching rate with small amount of fluorocarbon gas. In addition, reduction in fluorocarbon reduces etching rate of the Si-rich SiCN-cap, resulting in high selectivity in the via opening step.

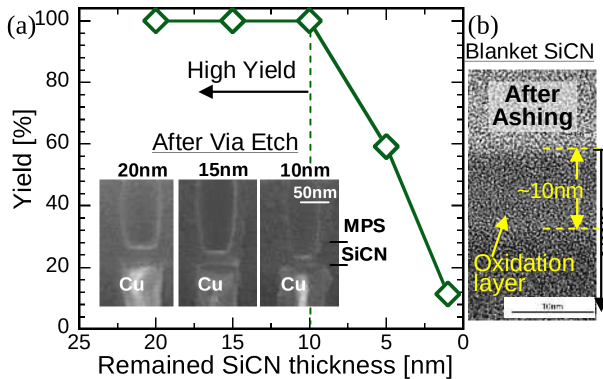

Fig.6 Dependence of via yield on the remained SiCN thickness after the via etching step. Oxide in the ashing ambient penetrate into the SiCN up to 10nm from the surface (TEM image in the right), resulting in yield loss due to oxidation of underlying Cu surface in the Cu-DD interconnects.

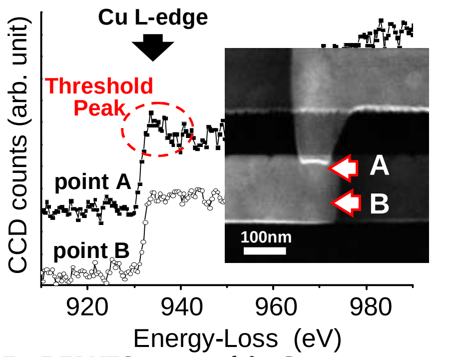

Fig.7 ELNES spectra of the Cu interconnect, in which the remained SiCN after the via-etch is nearly zero. Threshold peak of the Cu L-edge in the point A indicates that Cu surface just below the via is oxidized.

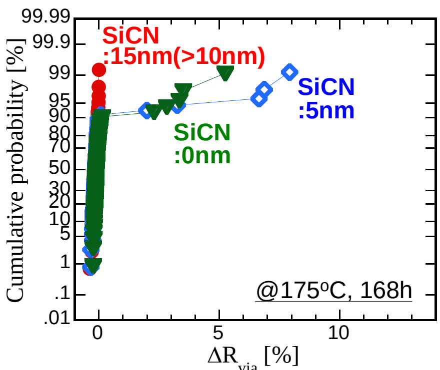

Fig.8 Shift of via resistance after a SiV test at 175°C for 168H for the samples with various remained SiCN thickness after the via etching step.

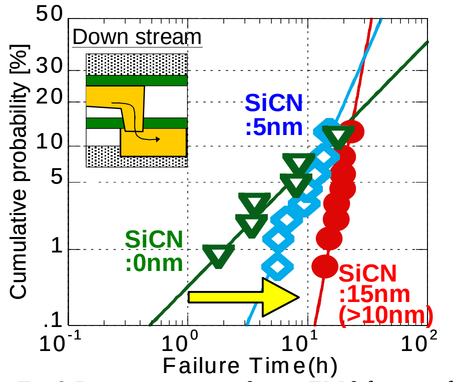

Fig.9 Down stream mode via-EM lifetime of the samples with various remained SiCN thickness. Early failure mode is eliminated by increasing the remained thickness.