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Cu Alloys and Noble Metal Liner Materials to Extend Damascene Cu Schemes

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1. Introduction

As the CMOS device dimensions shrink, the gap fill with Cu by electroplating becomes more difficult in Cu BEOL. Also, Cu BEOL systems face to reliability impacts, especially in electromigration (EM). Although our damascene scheme has been successful since the onset through five generations by using PVD-TaN/Ta as the liner material and PVD-pure-Cu seed, increase in the current density in finer volume of Cu and the finer trench/via formed in ultra low-k materials lead us to crisis in EM reliability and void-free Cu gap fill unless new technology elements are introduced such as CoWP metal capping, Cu alloys (CuAl, CuMn) and new alternative liner materials (Ru [1], Co [2]) which allow electroplating of Cu directly on them. However, introduction of such new materials tends to add new challenges and drawbacks. Electroless-plated CoWP capping, which improves EM by replacing the fast diffusion path of dielectric cap/Cu interface to CoWP/Cu interface, has to go over TDDB reliability issues so as to be implemented in manufacturing. So do the selective CVD-Co and CVD-Ru capping schemes. Cu alloys such as Al, Mn and Ti, known to improve EM, cause increase in line resistance (R). Alternative liner materials such as PVD-Ru(Ta), CVD-Ru, and CVD-Co, which improve Cu gap filling, add difficulties in defect-free CMP and increase in line R because the volume of Cu is reduced. Therefore, the process integration has to choose such new technology elements by balancing reliability, manufacturability, production cost, and penalty in Cu line R.

In this work, CVD Co film is characterized and its applicability as a seed enhancement layer to 22 nm integrations is discussed, followed by a preliminary work on Cu alloy PVD.

2. CVD-Co Film Properties and Process Integration

Cobalt films were deposited by CVD in a 300 mm wafer PVD/CVD cluster tool, using a dicobalt hexacarbonyl t-butylacetylene (CCTBA) precursor [2] followed by H_2 plasma post-treatment. CVD-Co films demonstrated the diffusion barrier function in the TVS (triangular voltage sweep) test (Fig. 1), but did not work as a barrier to O_2/moisture diffusion in the barrier oxidation test. This is a remarkable difference from PVD-RuTa(N) which did not work as a Cu diffusion barrier [1]. Fig. 2 shows AES profiles of PVD-Ta(N)/CVD-Co/PVD-Cu stacks. Incorporation of C and O

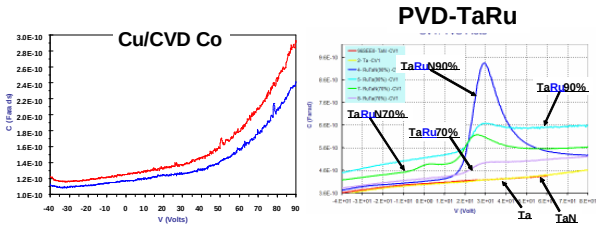


Fig. 1 TVS of CVD-Co, PVD-TaRu and TaN [6, 8]

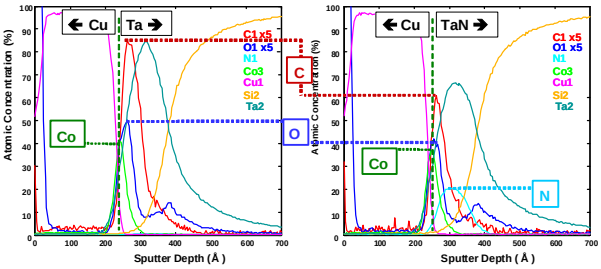


Fig. 2 AES profiles of PVD-Cu/CVD-Co on PVD-Ta and TaN

was less in CVD-Co formed on PVD-TaN than Ta. Decomposition of the Co precursor which contains carbonyl has been identified as the cause of the impurity incorporation through a further study on the dependency of impurity incorporation on underlying substrates such as PVD-Ru [2].

Fig. 3 shows XPS signals for O1s of Co as a function of ambient exposure time to show evolution of Co native oxide in the air. After 2 hr. exposure, the O1s counts reached almost the same level as that of the as deposited Co after 72 hrs in the air.

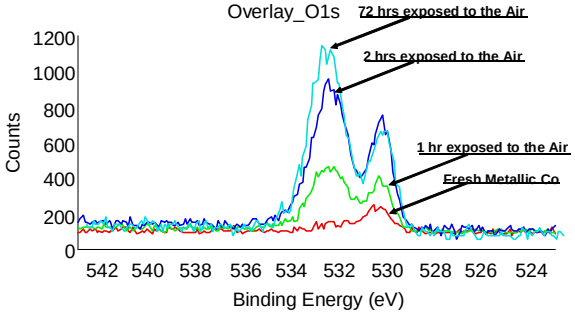


Fig. 3. XPS for O1s of CVD Co as a function of air exposure time.

This suggests evolution of Co oxide proceeds rapidly within the first few hours, towards a saturated level. The XRF measurement of Co thickness before and after direct plating of Cu in Fig. 4 suggests about 2nm thick Co layer is lost during Cu plating in the electroplating bath regardless of queue time from CVD-Co to plating. The rapid growth of Co native oxide (Fig.3) could be responsible for the Co loss during the direct plating.

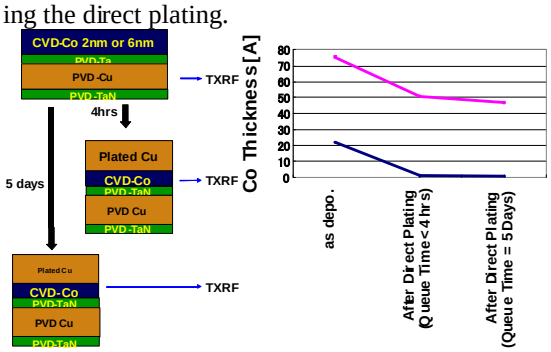


Fig. 4. XRF to show dissolution of Co in Cu plating bath during direct plating of Cu

Dual damascene Cu interconnects in k = 2.4 and 2.2 porous ULK SiCOH dielectrics were formed in 32 and 22 nm node dimension wiring. Based on the rapid oxidation of the CVD Co (Fig. 3), the liner/seed formation sequence used a PVD Cu seed to protect the Co prior to plating. The PVD TaN/CVD-Co stack was chosen based on several reasons: TaN is needed since CVD-Co is an inadequate barrier to O_2; Co on TaN (as opposed to Ta) showed reduced C and O incorporation (Fig. 2), and improved Cu texture Co on TaN [2].

Fig. 5 shows post-CMP top-down SEM images of 22 nm node dense Cu wiring. Cu-gapfill void formation seen on TaN wafers is not present for wafers with CVD-Co, suggesting improved Cu seed wettability and plating nucleation. This indicates that, at trench entrance locations where the Cu step coverage is apt to be insufficient, the Co is protected by the Cu cap and works as a plating enhancement layer.

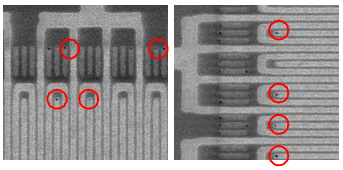


Fig.5a PVD-TaN/Ta

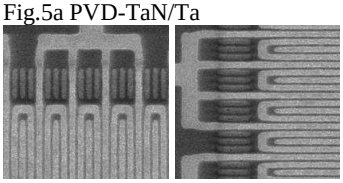


Fig.5b TaN/CVD-Co

Fig. 5. Post CMP defects for Cu lines with liner structures of PVD-TaN/Ta/Cu and with PVD TaN/CVD-Co/PVD-Cu.

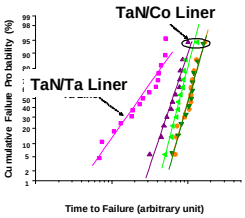


Fig. 6 EM Performance

Fig. 6 shows EM performance for electron flow from M2 through V1 to M1 in 32 nm node wiring. More than 7 times longer EM lifetimes are obtained with the PVD-TaN/CVD-Co liner compared to TaN/Ta. The reason for this EM improvement could be associated with the reduced defect formation in Fig. 5.

However, this advantage of CVD-Co in EM is lost when slit voiding at trench corners shown in Fig. 7 occurs. The worse EM performance is seen when the slit void is created. EDX/EELS profiles of Co, Ta and Co in Fig. 7 at trench corners show the absence of Co along the TaN sidewall at the slit. Since Co is less noble than Cu, it is Co which dissolves at the contact of Cu/Co. The Cu at the corner probably dissolves next after the Co disappearance.

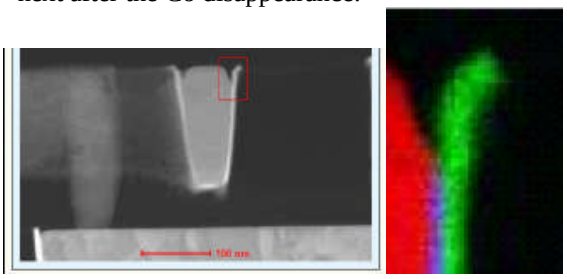
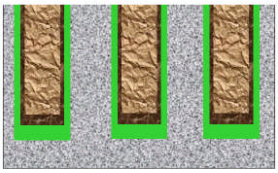


Fig. 7 Slit void and EELS/EDX profiles of Cu (red), Co (blue) and Ta (green)

3. CuAl-PVD into trench geometry

Fig. 8 shows the SIMS profile of Al in the CuAl0.5at% PVD seed layer. After Cu plating, CMP was performed without post-plating annealing to preserve the Al distribution in the Cu seed to see how the Al atoms are incorporated in the sputtered CuAl seed layer. Al atom counts are flat along the trench sidewall and are approximately double at the trench bottom. This is a basis for the impurity redistribution to be optimized through integration work to balance and achieve EM reliability and lower line R.



72nm line/space array

PVD TaN/Ta/CuAl0.5at%
➔ Cu Plating
➔no Annealing
➔➔ CMP

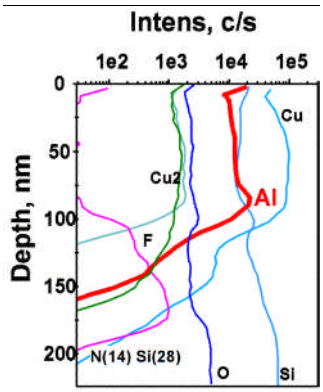


Fig. 8 SIMS profile of Al in trench geometry

4. Conclusions

CVD-Co films were characterized in terms of diffusion barrier properties to O_2/Cu, and O/C incorporation. A possible cause of loss of 2nm thick Co during direct Cu plating is the rapid evolution of Co native oxide. Based on these film characteristics of Co, the liner/seed stack of PVD-TaN/ CVD -Co/PVD-Cu was adopted to 32 nm and 22 nm dual damascene Cu/ULK BEOL to produce reduced post-CMP defectivity and improved EM performance. However, the advantage in EM is lost when the divot due to corrosion is formed at the entrance of trenches. CVD Co may have a promise in 22nm BEOL and beyond. There are also potential problems which need further investigations.

Acknowledgement

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References

[1] T. Nogami, *et al.*, Adv. Metal. Conf., 139, (2008).
[2] T. Nogami, *et al.*, IEEE IITC 3-1, (2010).