Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1190-1191

H-6-3(Invited)

The Effects of Pre-existing Voids on Electromigration Lifetime Scaling

C.V. Thompson

Massachusetts Institute of Technology
Cambridge, MA 02139 USA
Phone: +1-617-253-7652, E-mail: cthomp@mit.edu

I. Introduction

The 2009 ITRS indicates that there are no known solutions for achieving the reliability needed at the 18nm node and beyond. Among the approaches to addressing this problem are development of improved methods for optimizing, assessing, and predicting of the reliability of copper-based interconnects. This has driven development of improved simulations of electromigration and stress-induced failure, in order to more accurately scale test results to in-service conditions. It has also driven development of design rules and layout methodologies that account for beneficial effects deriving from the use of short interconnect segments. If these approaches are to be safely adopted, it is critical that assumptions about void growth and dynamics be experimentally validated, and modified as appropriate.

II. Current Density Scaling and Length Effects

Electromigration is a current-induced atomic flux that leads to an evolution in the mechanical stress in an interconnect segment at locations at which the flux is reduced or stopped, such as vias with liners. These mechanical stresses can lead to the nucleation of voids, and, once nucleated, electromigration leads to void growth, and often, void motion. Electromigration can also lead to growth of pre-existing voids that are present due to stress or processing defects.

Micro-scale current-induced stress evolution can be accounted for using the model developed by Korhonen et al [1], in which the time evolution of the local hydrostatic stress, σ, at a position x along the length of an interconnect can be calculated, with results such as those shown in Fig. 1.

Typically, x is set to zero at a location at which the atomic flux is zero, such as a via with a liner [Fig. 1, upper]. If x=0 at the cathode end of a segment the stress builds up over time with a maximum, σ_{max}, at x=0. σ_{max} reaches the critical value required for void nucleation, σ_{nuc}, at a time, t_{nuc}, that scales with j^{-2}. Once nucleation has occurred, the rate of void growth scales with j^{-1}. If growth to a critical void volume V_{crit} is required for failure [Fig. 1, lower] and it is assumed that the lifetime, t_f , scales simply j^{-n}, fitting of failure data will lead to a value of n ranging from 2 to 1, depending on whether void nucleation or void growth, respectively, dominates in defining t_f. If there is a pre-existing void, t_f will scale with j^{-1}.

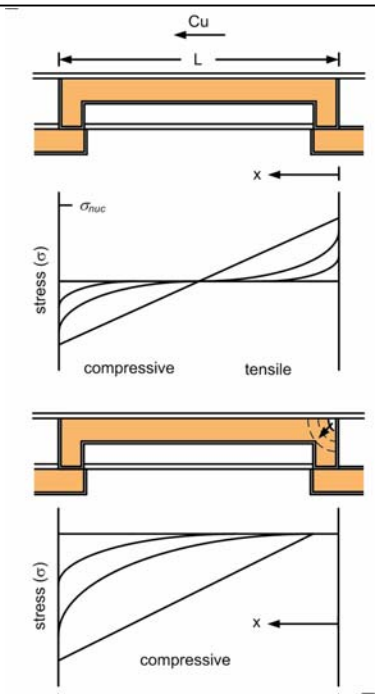

Fig.1: Upper, stress evolution prior to void nucleation. Lower, stress evolution during void growth.

For interconnect segments with blocking vias at both ends, a compressive stress develops at the anode and a tensile stress develops at the cathode. Eventually a stress gradient will develop that causes a back-stress force that opposes the electron-wind force, and stress at the anode and cathode will stop changing. If this occurs before failure, e.g. before σ_{max} is reached, the interconnect segment will be 'immortal'. In this case, there is a critical product of the current density and the segment length, jL, below which a segment will be immortal [2]. Interconnect structures can be laid out in such a way as to take advantage of this phenomenon to optimize circuit-level reliability [3]. It is often assumed that $(jL)_{crit}$ is defined as the time to reach σ_{nuc}. However, in the case of a low barrier to void nucleation or when there are pre-existing voids, $(jL)_{crit}$ will be defined by the time required to

reach V_{crit} [4]. It is always the case that $(jL)_{crit,\ growth} < (jL)_{crit,\ nuc}$. Accelerated testing makes it more likely that $(jL)_{crit,nuc}$ is what is measured, even when $(jL)_{crit,growth}$ is the relevant value for layout optimization and circuit-level reliability assessment.

III. Void Dynamics and Pre-Existing Voids

In the preceding discussion it has been implicitly assumed that void nucleation occurs at x=0. However, recent in-situ electromigration experiments have shown that voids often first appear at a distance, x>0 [5, 6]. These voids can grow in-place (at grain boundaries), break-free and drift toward the anode, be pinned at a grain boundary and grow some more, and break-free to drift to the anode where they grow until failure occurs [Fig 2]. Failure can also occur when the void is pinned at x>0. When this dynamic behavior occurs, current-density scaling is complex. As before, void nucleation and void growth scale as j^{-2} and j^{-1}, respectively. While void drift also scales with j^{-1}, depinning scales with $j^{-1/2}$ [7, 8]. Therefore, current density scaling is complex. Also, when voids first appear at a distance from the cathode, where the stress is not maximum, it is likely that voids pre-existed.

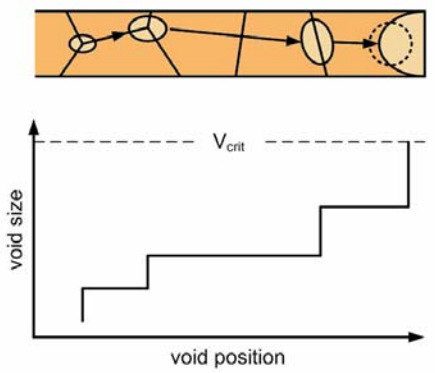

Fig. 2: Voids form, drift, become pinned and depin at grain boundaries. They can also drift across grains and grow at the cathode.

It should be noted that grain structures play an important role in the behavior outlined above. Voids first appear and grow at grain boundaries and they drift at the highest rates along grain boundary paths parallel to the interconnect lengths. Drifting voids can also become trapped at grain boundaries, where they grow until, or unless, they depin. As interconnect widths have decreased and aspect ratios have increased, grain sizes have decreased and optimum bamboo structures have become more difficult to attain.

Stress voids are common in copper technology and voids that undergo electromigration-induced growth at a distance from the cathode must be pre-existing. The critical void size (for which there is no barrier to growth) is ~1nm [8Nix], so that even high resolution microcopy is unlikely to allow detection of the smallest pre-existing voids that still affect electromigration lifetimes. Given the relatively poor adhesion to dielectric overlayers, it would be surprising if nm-scale voids *did not* exist at the Cu-dielectric interfaces. While estimates of the critical stress for void nucleation, σ_{nuc} are ~1GPa [9], and measured values of σ_{crit} for Al technology are ~0.5GPa, measured values of $(jL)_{crit}$ indicate a critical stress for void nucleation of 10's of MPa in Cu technology [10], which indicates little or no barrier to nucleation. Finally, if voids are present in a relatively small number of segments, their effects might go undetected in conventional electromigration testing, even though they would have a profound impact on in-service circuit-level reliability [11].

IV. Discussion and Conclusions

Ideally, pre-existing voids should be eliminated. The use of capping layers with better Cu adhesion would make this more probable. Obtaining bamboo grain structures would reduce the probability of void formation, reduce the rate of void drift, and decrease void pinning. These idealities have been difficult to achieve. Use of reservoirs at cathodes (horizontal or vertical extensions of the segment beyond the via) to allow for increased void growth before failure (increased V_{crit}) in likely to improve lifetimes. Layout strategies that rely on improved reliability in short lines will still allow optimization of circuit-level reliability, but the effects of pre-existing voids on $(jL)_{crit}$ must be accounted for. Finally, when voids are pre-existing, current-density scaling is complex, and new data analysis procedures are needed.

References

[1] M.A. Korhonen, P. Borgesen, K.N. Tu, and C.Y. Li, J. Appl. Phys. **73**, (1993) 3790.
[2] I.A. Blech, J. Appl. Phys. **47**(1976) 1203.
[3] J.J. Clement, S.P. Riege, R. Cvijetic, and C.V. Thompson, IEEE Trans. on CAD of Int. Circ. and Sys. **18**, (1969) 576.
[4] R.G. Filippi, R.A. Wachnick, H. Aochi, J.R. Lloyd, M.A. Korhonen, Appl. Phys. Lett. **69**, (1996) 2350.
[5] M.A. Meyer, M. Herrmann, E. Langer, E. Zschech, Microelec. Eng. **64**, p375 (2002)
[6] Z.-S. Choi et al, J. Mater. Res. **23,** (2008) 383.
[7] P. Børgesen, M.A. Korhonen, D.D. Brown, and C.Y. Li, AIP Conf. Proc. **263**, (1992) 219.
[8] T. V. Zaporozhets et al, J. Appl. Phys. **98**, (2005).
[9] R. J. Gleixner, B. M. Clemens, and W. D. Nix, J. Mater. Res. **12**, (1997) 2081.
[11] C.S. Hau-Riege, A.P. Marathe, V. Pham, Adv. Met. Conf., (2002) 169.
[12] S.P.Hau-Riege, J. Appl. Phys. **91**, (2002) 2014.