Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp1194-1195

3D Integration Technology and 3D System-on- a Chip

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1. Introduction

Recently three-dimensional (3D) integration technology using through-Si vias (TSVs) as shown in Fig.1 has attracted much attention since it gives rise to the higher packing density, shorter interconnections, lower power consumption and heterogeneous device integration[1)-8)]. We have previously reported 3D integration technology using wafer-to-wafer bonding[1)-5)] and fabricated several prototype 3D LSI test chips [9)-12)]. In the wafer-to-wafer 3D integration technology, however, the overall chip yield exponentially decreases with an increase in the number of stacked layers as summarized in Table 1. On the other hand, the inherent problem in the chip-to-wafer 3D integration technology is the low production through-put. To solve these problems, we have proposed a new super-chip integration technology based on the reconfigured wafer-to-wafer bonding and multichip-to-wafer bonding [13)]. Many chips are simultaneously aligned and bonded with high alignment accuracy using a self-assembly technique in a super-chip integration technology. We describe such a super-chip integration technology in this paper.

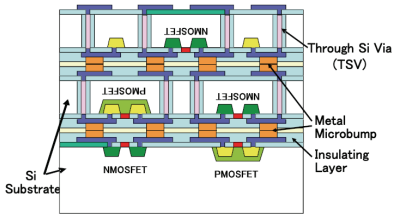


Fig.1 Cross-sectional structure of 3-D LSI.

Table 1 Stacking methods for 3D integration

Stacking methods	Chip-to-chip	Chip-to-wafer	Wafer-to-wafer	Self-assembled chip-to-wafer
Production throughput	Extremely Low	Low (pick & place)	High	High (self-assembly)
Production yield	High	High	Low	High

2. Super-Chip Integration Technology

A number of known good dies (KGDs) are simultaneously aligned and bonded onto lower chips or wafers with high alignment accuracy using a self-assembly technique in a super-chip integration technology. Fig.2 describes the concept of super-chip integration. After wafer probing and dicing, many KGDs with TSVs are simultaneously aligned and temporarily bonded to a supporting wafer to fabricate a reconfigured wafer. Then KGDs in a reconfigured wafer are thinned from the backside by the mechanical grinding and chemical mechanical polishing (CMP) to expose the base of TSV's after coating a high-viscosity resin. After that, the metal microbumps are formed onto the base of TSV's. This reconfigured wafer with many thinned KGDs is firmly bonded to another reconfigured wafer and then the supporting wafer of the upper reconfigured wafer is removed. By repeating these sequences, we can obtain 3D LSI chips with several chip layers. We can fabricate a new 3D LSI called a super-chip as shown in Fig.3 by using the super-chip integration technology.

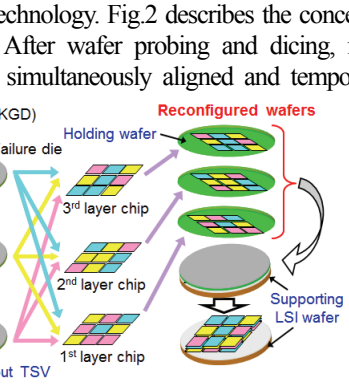


Fig.2 3D LSI fabrication by super-chip integration technology.

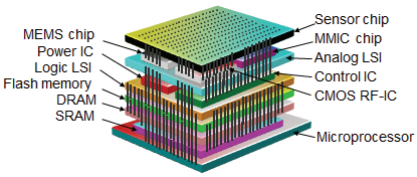


Fig.3 Conceptual structure of 3D super-chip.

3. Chip Self-Assembly

A chip self-assembly is the key in our super-chip integration technology. The chip self-assembly process using a small volume of aqueous solution is schematically shown in Fig.4. First, a thin silicon dioxide layer is formed on a Si wafer. Then, hydrophilic areas are photolithographically patterned on the Si wafer, followed by the formation of hydrophobic areas surrounding the hydrophilic areas. After that, aqueous solutions are dropped onto the hydrophilic areas. Subsequently, many Si chips with the hydrophilic backside are roughly aligned on the hydrophilic bonding areas and then placed on them. Immediately after the chip placement, the Si chips are simultaneously and precisely aligned on the hydrophilic areas in a short time. Finally, these Si chips are tightly bonded on the hydrophilic areas after the liquids are evaporated at room temperature. We confirmed by a self-assembly experiments that it takes less than 0.6 sec to completely align the chips by surface tension of aqueous solution and obtained the average alignment accuracy of 0.43um. We have developed a new self-assembly machine for 8-inch wafer. More than 500 KGDs were simultaneously bonded onto a holding wafer by using this machine as shown in Fig.5. We have fabricated 3D LSI test chips by the reconfigured wafer-to-wafer bonding using the self-assembly technique. Fig.6 shows photographs after stacking three layers of KGDs. It is obvious that KGDs with different die sizes are stacked with high alignment accuracy. It is possible to stack different kinds of chips on LSI

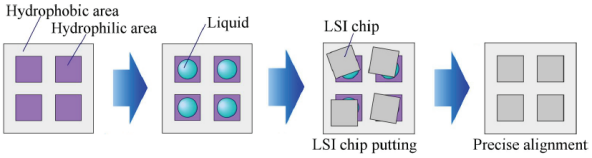


Fig.4 Process sequence for self-assembly on Si

using the self-assembly technique. Fig.7 shows a photo-micrograph of MEMS pressure sensor chip stacked on an LSI chip using the self-assembly technique. The LSI chip was bonded to the silicon substrate also using the self-assembly technique and Cu wirings were directly formed onto this chip and the substrate.

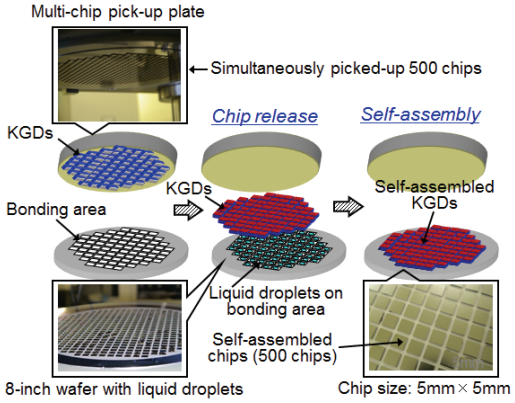
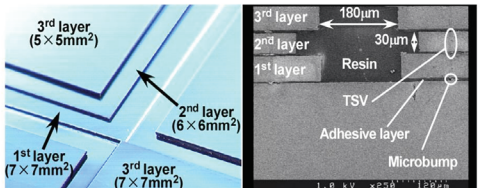


Fig.5 Self-assembly process using a self-assembly machine for 8-inch wafer.



(a) (b)

Fig.6 Photomicrograph of plan view (a) and SEM micrograph of cross-sectional view (b) of 3D test chips with different chip sizes.

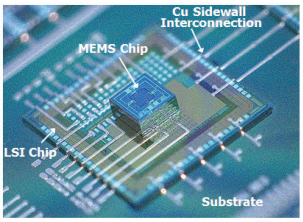
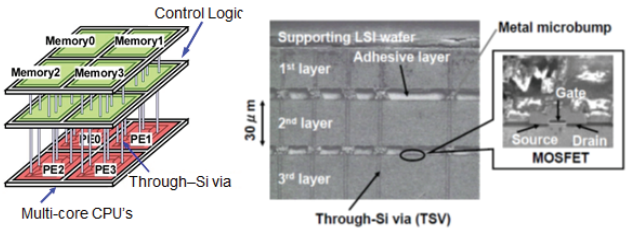


Fig.7 Vertically stacked MEMS chip on LSI chip by self-assembly.

4. Three-Dimensional System-on-a Chip (3D-SoC)

We can create various kinds of new SoC's with parallel processing and parallel data transferring capabilities by employing 3D stacked structures having many TSV's. Typical one of these new 3D-SoC's is 3D microprocessor in which several memory layers are stacked on a microprocessor chip. Extremely wide data bandwidth of more than Tera-bytes/s can be achievable between a processor chip and stacked memory chips. We have fabricated a 3D microprocessor test chip as shown in Fig.8 to confirm vertical data transfer and basic arithmetic function through TSV's. It was confirmed in this test chip that data read from the SRAM cache memory in the third layer were transferred to the processor in the first layer through the second layer to successfully perform the arithmetic operation. Another example of new 3D SoC's is a 3D-stacked image processor chip as shown in Fig.9 where image sensor chip, ADC chip, image processor chip and memory chips are vertically stacked. Several thousands of ADC's simultaneously operate in parallel to achieve an extremely high data conversion rate and high frame rate of more than 10,000 frames/s for image processing in this 3D-stacked chip. A highly dependable SoC with 3D-stacked structure as shown in Fig.10 is also another example of new 3D-SoC's where a self-repair and redundancy circuit layer and a test circuit layer with BIST and scan path circuits are inserted between a processor chip and memory chips. In this 3D-SoC, real-time testing is performed in the test circuit layer and failure circuits are replaced by self-repair and redundant circuits in the self-repair redundancy circuit layer to achieve a higher dependability.



(a) (b)

Fig.8 Configuration of 3-D microprocessor test chip (a) and SEM cross-sectional view of it (b).

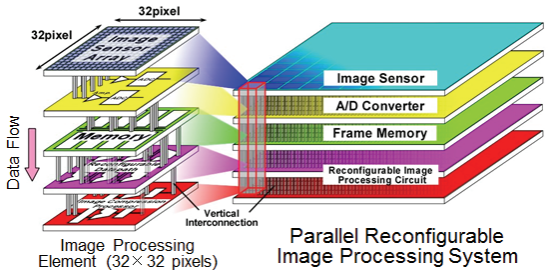


Fig.9 Configuration of 3D-satcked image processor.

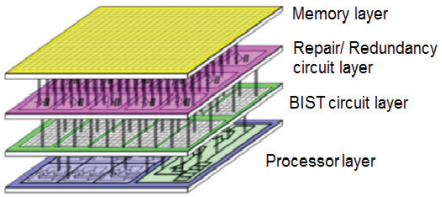


Fig.10 Configuration of 3D-SoC with self-test and self-repair function.

5. Summary

We have developed a new 3D integration technology based on a reconfigured wafer-to-wafer bonding method called a super-chip integration. In addition, we have proposed and discussed new 3D-SoCs such as a 3D microprocessor, 3D-stacked image processor and 3D dependable SoC.

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