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Evaluation of Copper Diffusion in Thinned Wafer with Extrinsic Gettering for 3D-LSI by Capacitance-Time (C-t) measurement

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1. Introduction

In recent, multiple stacked 3-D LSI applications are targeted, integrating processor, memory, sensor, logic, analog, power ICs and wide-bands ICs into one chip that will be used in future cell phones, super-computers, network / storage systems, notebooks, automotive and medical processing units. Because a 3D integration technology offer a very attractive challenge to realize the higher transistor density, faster interconnections, heterogeneous technology integration, and potentially lower cost and short time-to-market.

Wafer thinning and formation of through-Si via (TSV) and metal microbump are key processes in 3D LSI fabrication [1, 2]. Wafer thinning of less than 10 μm is technologically possible, however, the device performance of the thinned wafer would be seriously damaged by backside grinding and the following chemical mechanical polishing (CMP) due to their mechanical stress. In addition, Cu is extensively used in TSVs, metal microbumps and lateral interconnects. Generally, Cu and Au rapidly diffuse in Si substrate at relatively low temperature. Also, the device performance of the thinned wafers would be also affected by the back end of line (BEOL) processes due to the metallic contamination even though the processes are proceeded at below 300 ºC. Cu in Si substrate seriously degrades the carrier lifetime and hence the device characteristics [3, 4].

An important parameter when specifying highly pure Si is the minority carrier generation lifetime. Minority charge carriers in Si recombine at crystal defects, surface damage or deep levels created by metal impurities. Capacitance-time (C-t) analysis and Zerbst method are highly sensitive and promising candidates for measuring very short generation lifetime which is caused by the metallic contamination and the crystal defects. Therefore, the analysis of metallic contamination and device reliability for the 3D integration has been attracted much attention in recent years. To suppress such metallic impurity diffusion, intrinsic gettering (IG) and extrinsic gettering (EG) are very important as shown in Fig.1.

By the grinding conditions, the thickness of the defect band is strongly affected and is between 0.1μm and about 1 μm. The residual defects layer has a similar gettering layer formation mechanism. And the residual defects layer formed during mechanical grinding and stress-relief processes is also useful as a gettering layer.

In this paper, we have investigated MOS capacitor fabricated on thinned p/p- wafer by C-t method and Zerbst method and evaluated the effect of EG layers against metallic contamination which are formed by the backside grinding and the following CMP, the dry polishing (DP) and the ultra-poligrind (UPG) methods. Furthermore, comparison of the effects of gettering layers in thinned p/p- and p/p+ wafer, which is formed by wafer thinning process, has been evaluated by using the capacitance transient characteristics.

2. Experimental

MOS structures on the p/p- and p/p+ silicon wafer were fabricated after thinning wafer using the backside grinding and the following CMP, DP and UPG method as shown in Fig. 2. The surface morphology, the mechanical stress and crystal defects of backside of thinned wafers were evaluated by Atomic force microscopy (AFM), micro-Raman spectroscopy (μ-RS), and transmission electron microscopy (TEM), respectively. After the formation of 10nm gate oxide, 800 nm thick Al electrodes are evaporated to fabricate the MOS structure. Then H_2 annealing was performed at 450 ^oC for 30min and a 100-nm-thick Cu was evaporated on the back side of the thinned wafers. After that, the wafers were annealed at 300 ºC in N_2 ambient for various annealing time to introduce a metallic impurity contamination into the silicon substrate. The C-t measurements were performed using Agilent B1500A semiconductor device parameter analyzer. Electron-hole pair generation in the space charge region is dominant when the MOS device is measured using C-t measurement at room temperature.

3. Results and Discussion

The thickness of the defect band is strongly affected by the grinding conditions, and is between 0.1μm and about 1 μm as shown in Fig. 3. Also, the surface morphology on the back-side of thinned wafers with grinding and the following CMP, DP and UPG method were evaluated by using AFM. As shown in Fig. 4, a roughness of thinned silicon wafers using CMP, DP, and UPG is about 0.3 nm, 2 nm, and 8 nm, respectively. It is clear that UPG does not have a positive effect on the surface roughness improvement. In fact, the UPG produced a much coarser surface, as demonstrated by a roughness comparison among the surfaces treated by CMP, DP and UPG. The process may also create sub-surface damage to the silicon wafer like disordering, point defect and dislocations in Si crystal and vertical micro-cracks that induce wafer stress. In order to evaluate the stress/strain distribution, we have carried out 2D- μ-RS imaging of on CMP, DP and UPG treated wafers and the data are shown in Fig. 5. From the results, it is clear that the stress/strain distribution in the CMP treated wafer is quite low as compared to both the DP and UPG process. Although the roughness of UPG treated wafer is relatively larger than that of DP and CMP treated wafer, however, the stress/strain distribution in the UPG treated wafer is similar to that in the DP treated wafer. Therefore, to evaluate the EG effect against metal contamination and to analyze the performance of MOS capacitor fabricated on the thinned p/p- and p/p+ wafer, the C-t method is introduced. Figures 6 and 7 show the measured C-t plots of MOS capacitor on the thinned p/p- and p/p+ wafer using CMP, DP, and UPG before and after Cu diffusion at 300^{o}C for 60min. The Al electrode had a circular shape with ϕ = 500 μm and the substrate concentration is N_d=1.0×10^{15} /cm^3. The Zerbst plot represents the generation of the inversion charge Q_{inv}, which is proportional to the time derivative -d(C_{ox}/C)^2/dt. The time derivative -d(C_{ox}/C)^2/dt is plotted as a function of C_f /C-1, which is the normalized effective depth in Figs. 8 and 9, where the C_{ox} is the oxide capacitance, C_f is the steady-state capacitance in the inversion condition and measured C is the high frequency capacitance, respectively. The slope of the so-called Zerbst plot -d(C_{ox}/C)^2/dt versus C_f/C-1 gives the generation lifetime τ_g of minority carriers. The initial τ_g's of p/p- wafer with UPG, DP and CMP treatments are about 1537 μs, 1528 μs and 1288 μs, respectively. And also the initial τ_g's of p/p+ wafer with UPG, DP and CMP treatment are about 1517 μs, 1607 μs and 2400 μs, respectively. In Figs. 10 and 11, normalized τ_g versus annealing time at 300^{o}C are plotted for different p/p- and p/p+ wafers and different thinning processes. In the p/p- wafer with CMP treatment, τ_g is significantly decreased by Cu diffusion at 300^{o}C for 60 min. However, the DP treated p/p- wafer shows the strong immunity to Cu contamination. The effects of employing the p/p+ wafer with same treatments on Cu contamination are described Fig. 11. It was shown that the p/p+ wafer is effective to suppress the Cu diffusion in the CMP treated wafer. Furthermore, it was suggested that the point defects/dislocation defects formed near the grinded surface of DP treated wafer can act as an EG layer and however, the UPG treated wafer with the deep micro-cracks and strong stress/strain contribution is relatively unstable.

4. Conclusions

The effects of EG layers formed on p/p- wafers and p/p+ wafers by backside grinding and the following CMP, DP and UPG methods against metallic contamination induced has been investigated. The behaviors of minority carrier generation lifetime in thinned p/p- and p/p+ wafer with UPG, DP and CMP treatments are evaluated by the C-t measurement and Zerbst plot. The gettering efficiency of DP treated p/p- and p/p+ wafer is enhanced about 50% as compared with CMP treated p/p- wafer and 19% as compared CMP treated p/p+ wafer, respectively. Thus we could succeed in quantitatively evaluate the gettering efficiency for Cu contamination by extracting the minority carrier lifetime in thinned wafers with different backside treatments and various thinning processes.

Acknowledgment

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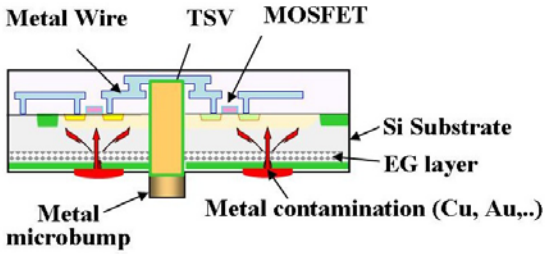

Fig. 1 Metal contamination in thinned Si wafer for 3D-LSI with extrinsic gettering(EG) layer.

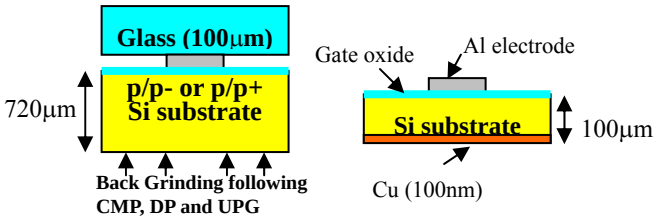

Fig. 2 MOS capacitor structures on the p/p- and p/p+ silicon wafer with thinning process.

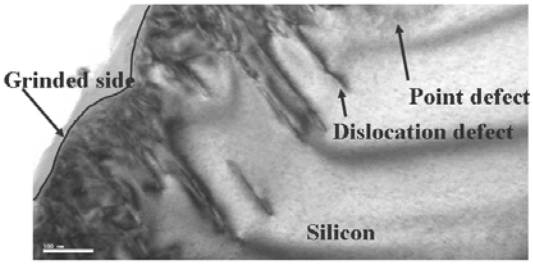

Fig. 3 Cross-sectional TEM image of defect structure near the surface after mechanical grinding.

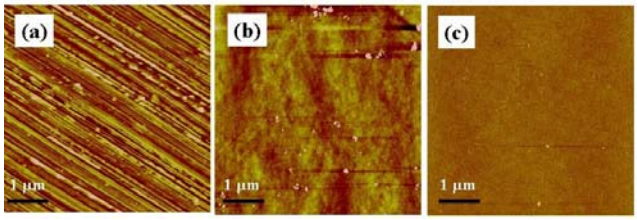

Fig. 4 AFM images of a silicon surface after mechanical grinding followed by UPG (a), DP (b), and CMP (c).

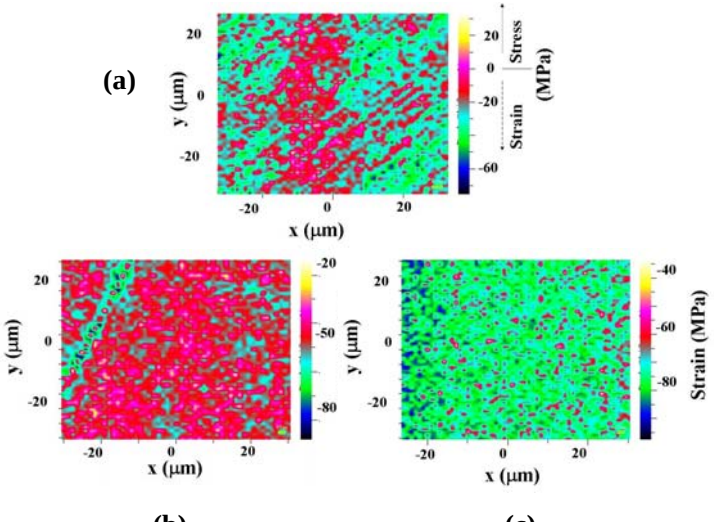

Fig. 5 μ-Raman mapping images of a silicon surface after mechanical grinding followed by UPG (a), DP (b), and CMP (c).

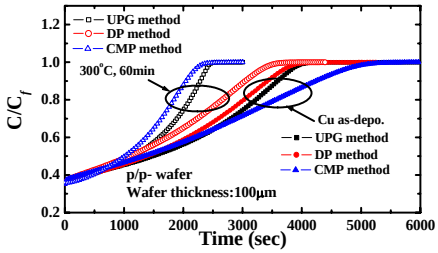

Fig. 6 C-t plots of MOS capacitor on the thinned p/p- wafer before and after Cu diffusion.

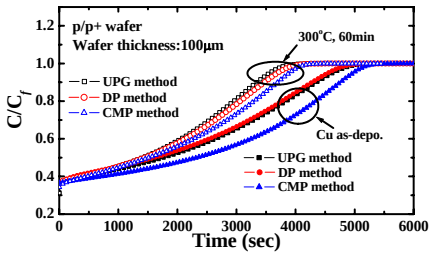

Fig. 7 C-t plots of MOS capacitor on the thinned p/p+ wafer before and after Cu diffusion.

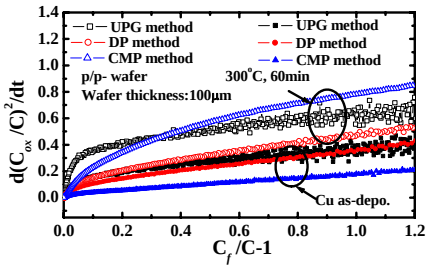

Fig. 8 Zerbst plots of MOS capacitor on the thinned p/p- wafer using CMP, DP, and UPG before and after Cu diffusion at 300°C for 60min.

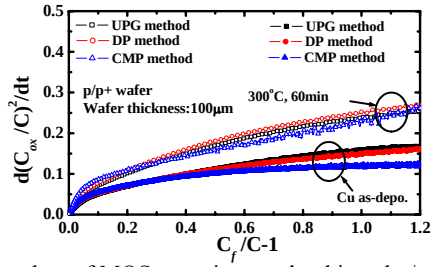

Fig. 9 Zerbst plots of MOS capacitor on the thinned p/p+ wafer using CMP, DP, and UPG before and after Cu diffusion at 300°C for 60min.

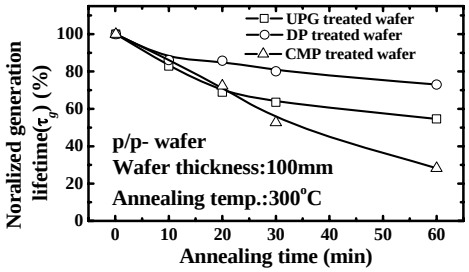

Fig. 10 Normalized τ_g in MOS capacitor on the p/p- wafer with various thinning process versus annealing time.

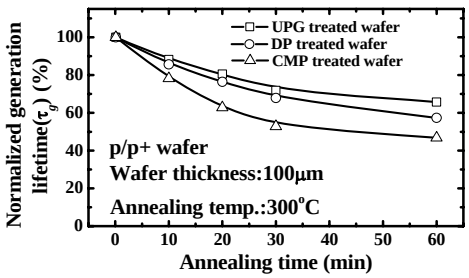

Fig. 11 Normalized τ_g in MOS capacitor on the p/p+ wafer with various thinning process versus annealing time.