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Self-Assembly with Metal Microbump-to-Microbump Bonding for Advanced Chip-to-Wafer 3D Integration

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1. Introduction

Through-Si vias (TSVs) and 3D chip stacking have recently attracted great attention to not only decrease chip size and shorten long global wirings but also significantly increase signal processing speed and dramatically decrease power consumption [1], [2]. 3D integration using wafer-to-wafer bonding is a promising technology due to its high production throughput. On the other hand, 3D integration using chip-to-wafer bonding can provide high production yield due to the use of known good dies (KGDs). However, conventional chip-to-wafer 3D integration technology decreases production throughput because robotic pick-and-place assembly of one-by-one chip stacking is employed. To overcome the problem, we proposed a new chip-to-wafer 3D integration technology based on a self-assembly technique using liquid surface tension by which a large number of KGDs can be simultaneously, rapidly, and precisely stacked on an LSI wafer in batch [3]-[6].

In this present paper, we demonstrate chip self-assembly with high-precision alignment and metal microbump-to-microbump bonding for advanced chip-to-wafer 3D integration. As shown in Fig.1, chips having arrays of metal microbumps are directly self-assembled in a flip-chip bonding manner to substrates that have the same microbump arrays. Here, we employed 5-, and 10-μm-size In/Au microbumps for the self-assembly experiments. This paper also describes the electrical characteristics obtained using microbump daisy chains formed between self-assembled chips and substrates.

2. Experimental

Arrays of In/Au microbumps were formed on chips and substrates in the following processes, as shown in Fig.2. First, Al/W wirings were formed on a thermally oxidized wafer by sputtering and reactive ion etching (RIE). Then, a plasma-TEOS (tetraethylorthosilicate) oxide layer was deposited by chemical vapor deposition (CVD) on the Al/W wirings, followed by contact hole formation by RIE. After that, metal microbumps consisting of 3-μm-thick In and 0.3-μm-thick Au were formed by our unique lift-off technique with RIE and evaporation [7]. The resulting chip size was 6 mm by 6 mm and the substrate size was 10 mm by 10 mm. The region around chip bonding areas was rendered hydrophobic by a surface modification technique with a thin fluorocarbon film. Finally, the chip were obtained by mechanical dicing.

In self-assembly processes, small droplets (approximately 2 μl) of aqueous liquid were provided onto hydrophilic bonding areas formed on substrates, and then, chips were roughly prealigned upside down to the bonding areas. Immediately after chip release, the chips were precisely self-aligned onto the bonding area by liquid surface tension as a driving force. After liquid evaporation at room temperature, the self-aligned chips were heated at 200˚C without mechanical compression to give flip-chip interconnections with metal microbump-to-microbump bonding. The alignment accuracy of the self-assembled chips to wafers was measured by observing vernier patterns formed on the surface of the chips and the substrates. The verniers can exhibit the resolution of ± 2 μm in *X* and *Y* directions.

3. Results and discussion

Figure 3 shows top views of the resulting chip and substrate in which three regions involving 10-μm-size In/Au microbump arrays formed on Al/W wirings can be observed: 100-, 150-, and 300-μm-pitch microbump arrays are formed in the right bottom, left bottom, and top regions, respectively. 200 In/Au microbumps exist in each region. Chips having 5-μm-size microbumps also have the same layout to the chips having 10-μm-size microbumps. In addition, vernier patterns are located on the left and right sides as shown in Fig.3. Figure 4 shows SEM views of 5- and 10-μm-size In/Au microbumps formed by our unique lift-off technique. The microbump height is approximately 3 μm.

Figure 5 shows contact angle measurement on the hydrophilic bonding area and the surrounding hydrophobic area formed on a substrate having 10-μm-size microbumps. The contact angle of the hydrophilic bonding area is 57 degree, whereas the contact angle of the surrounding hydrophobic area is more than 100 degree, which has high potential to precisely align chips to substrate because aqueous liquid is strongly confined to the central bonding area.

Figure 6 shows IR images of vernier patterns observed with transmitted light through a self-assembled Si chip and a substrate having In/Au microbumps. In any cases, the alignment accuracies are relatively high. From our experiments, it was noted that alignment accuracy intensively depends on initial misalignment before chip release, wettability contrast between hydrophilic and hydrophobic areas, and alignment error in dicing. By controlling and optimizing these conditions, the alignment accuracy would increase within 100 nm. Figure 7 shows *I-V* characteristics measured using 5- and 10-μm-size microbump daisy chain patterns. We have confirmed that contact resistance of the self-assembled chips to a wafer was similar to that obtained by conventional mechanical flip-chip bonding [6]. In this study, the contact resistances obtained from both microbump daisy chain patterns were relatively high due to the high contact resistance between microbumps and W layers. As seen from

the Fig.7, however, all microbumps (200 chain) are electrically connected using 10-μm-size microbumps. On the other hand, just two pair of microbumps are successfully bonded when 5-μm-size microbumps are used. The reason is not clearly understood, but alignment error in θ directions and partial oxidization of the microbumps by the liquid used in this study would affect the resulting electrical characteristics.

4. Conclusions

We demonstrated self-assembly of chips having metal microbumps with 5 and 10 μm in size onto substrates. All chips with the fine In/Au microbumps were successfully self-aligned with high alignment accuracy and bonded at 200 ˚C without mechanical compression. The self-assembly technology can be a high promising candidate for 3D integration based on KDGs-to-wafer stacking in batch.

Acknowledgements

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References

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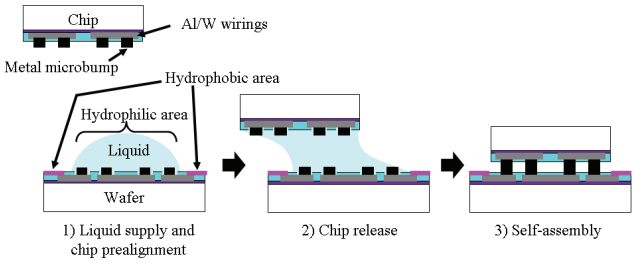


Fig.1 Chip self-assembly with microbump-to-microbump bonding for advanced chip-to-wafer 3D integration.

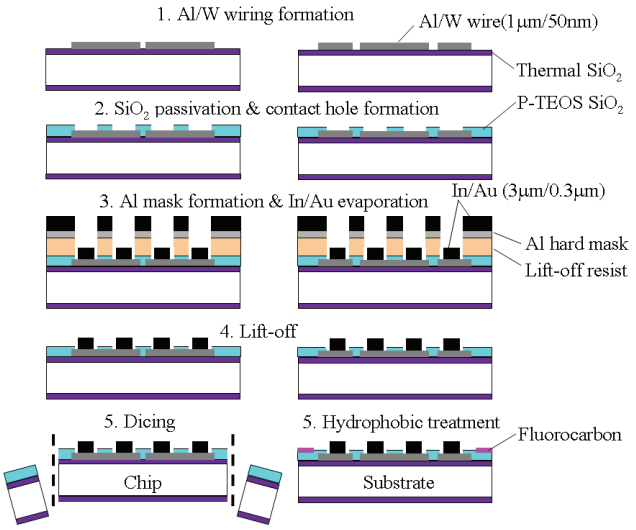


Fig.2 Process flows for chip (left) and substrate (right) fabrication for self-assembly.

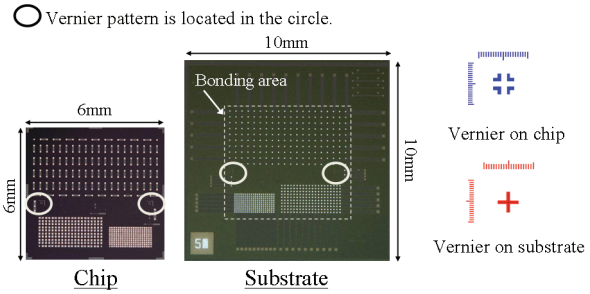
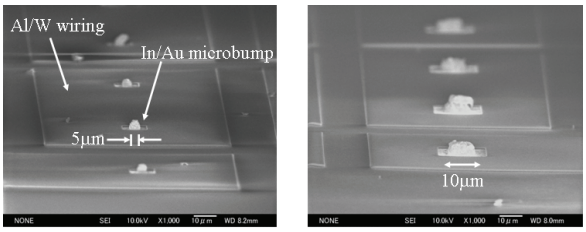


Fig.3 Photomicrographs (top view) of a fabricated chip and substrate having verniers and 10-μm-size microbump arrays.



(a) 5μm × 5μm microbumps (b) 10μm × 10μm microbumps

Fig.4 SEM of In/Au microbumps formed on Al/W wirings.

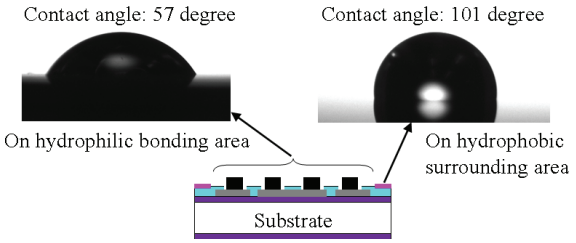
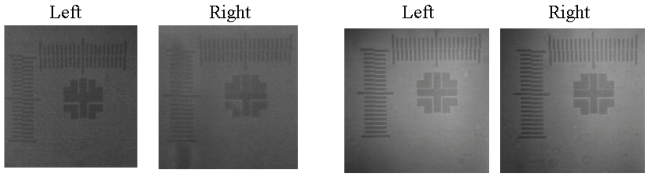
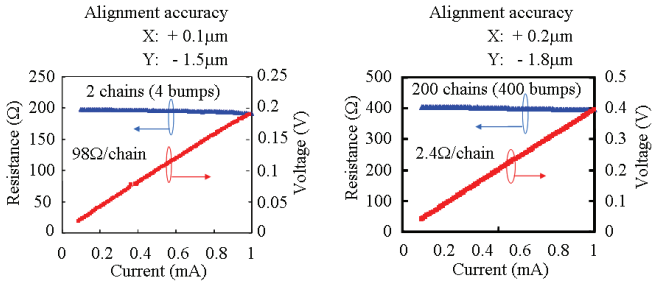


Fig.5 Contact angle measurement of hydrophilic bonding area and the hydrophobic surrounding area.



(a) Chip having 5μm × 5μm microbumps (b) Chip having 10μm × 10μm microbumps

Fig.6 IR images of vernier patterns obtained after chip self-assembly on substrates.



(a) Chip having 5μm × 5μm microbumps (b) Chip having 10μm × 10μm microbumps

Fig.7 *I-V* characteristics of bump contact resistance measured using In/Au microbump chain patterns formed by self-assembly.