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Metal Micro-Bump Induced Stress in 3D-LSIs _a micro-Raman Study

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1. Introduction

Recently, heterogeneous system integration involving CMOS, MEMS, optics, and biochips has attracted much attention due to its high functionality, potential applications and low power consumption. Fig. 1(a) shows a conceptual structure of hetero-integrated MEMS-LSI multi-chip module (MCM), which we have proposed earlier. In order to realize the MCM, we developed several key technologies such as multi-chip fluidic self-assembly, passive devices (which are interconnected via Cu-lateral interconnections) on a chip as shown in Fig. 1(b).[1] Shown in Fig. 1(c) is the schematic view of three dimensional (3D)-superchip which may obtained by stacking the MCMs vertically.

Among several interconnection methods employed in 3D-integration, high density micro-bump technology for flip-chip (face-up and face-down) bonding of die and the through Silicon via (TSV) for electrical connections are of key technologies. The Si die/wafer has to be thinned down to few tens of μm to fabricate 3D LSI, in order to improve the LSI performance and enhance the packaging density. However, this might introduce the mechanical stress and crystal defects in the Si substrate.[2] Further, the metal micro-bump bonded, thinned 3D-LSI wafer/die (as shown in fig. 4&6) might be under local mechanical stress/strain, introduced by difference in co-efficient of thermal expansion (CTE) between the metal of the micro-bump and the Si. This induces local mechanical stress in the thinned Si substrate and consequently changes the device characteristics.

In this work, we have mainly focused on the induced stress/strain in thinned 3D-LSI Si die/wafer by the metal micro-bumps. Micro-Raman spectroscopy (μRS) is a versatile tool to probe both the crystal quality and the remnant stress/strain (qualitative as well as quantitative) in the Si die/wafer.

2. Fabrication of Cu-Sn micro-bump on LSI

Fig. 2 shows the fabrication process of Cu-Sn micro-bump formation. We have developed a new bumping technology called EEB (electroplated- evaporation bumping) technology, where a 3 μm thick Cu bump is formed by electroplating which is followed by an evaporation of 2 μm thick pure Sn. Shown in Fig. 3 & 4 are the cross-sectional SEM image and the I-V characteristics of Cu-Sn micro-joint, respectively. Detailed results on bump characteristics can be found elsewhere.[3] After fillip-chip bonding, we have systematically analyzed the residual stress in 3D-LSI after die-to-wafer bonding via high density metal micro-bumps. To evaluate the stress distribution in such a micro-bump bonded LSIs on both the top surface (region between the micro-bumps) and the cross-section (region below the micro-bump), we have carried out 2D-μRS study. Various samples were analyzed for bump spacing, bump size, bonding temperature, and applied pressure during joint formation. The μR spectra were recorded at room temperature with a LabRam confocal microscope equipped with a charge coupled device detector using Ar+ 488 nm laser focused to a 1 μm spot (1.4 mW) and a 100X objective. The spectral resolution is around 0.4 cm^{-1}. From the Raman data, the stress/strain was calculated, as shown in Fig. 5.

3. Residual stress in bonded Si die/wafer

The bond forming process is performed at a relatively high temperature (in this study, it was 300 ℃). After the micro-joint formation, when the whole die-wafer cools down, the metallic micro-joint shrinks more than the Si die/wafer due to the difference in CTE (the CTE [in ppm/K] for Cu and Si are ~16.5 and ~2.6, respectively). *Consequently, the micro-joint will introduce compressive stress in the Si die/wafer.* In order to realize the 3D- superchip (Fig. 1(C)) with high I/O density, it has been required very fine-pitch small size micro bumps. *This fine-pitch micro-joint may further aggravate the stress introduction.*

Shown in Fig. 6 and 7 are respectively an optical image and the stress distribution (obtained from Raman shift) in 3D-LSI bonded with 400 μm² square size Cu-Sn micro-bump with 40 μm bump spacing. It is inferred that the Si (both die & wafer) immediately below the bump region is under compressive stress. The compressive stress decreases exponentially in the cross-sectional direction both at die and wafer. But, in the horizontal direction it vanished nearly abruptly, and nearly zero stress or relatively small tensile strain is noticed for bump spacing region at the die. This tensile stress is produced by the edges of the two adjacent micro-joints that pull the Si atoms together. This tensile stress is a crucial reliability issue, since it may induce cracks in the 3D-LSI die/wafer. It is worth noting that the stress distribution in 3D-LSI (in this study) die/wafer due to the metal micro-joint is nearly close to the stress distribution phenomenon observed for the Cu wire-bonded Si die.

To evaluate the role of finer bump-pitch on the stress distribution pattern, we have done the 2D-μR mapping study on bonded 3D-LSI die/wafer with 100 μm² square size Cu-Sn micro-bump with 10 μm bump spacing. In general, we observed a similar cross-sectional stress distribution pattern for both 20 μm and 10 μm bump spacing. On the other hand, for 10 μm bump-spacing, the compressive stress produced by the two adjacent micro-bumps overlapped to each other at the region of bump-spacing. Hence, for the 3D-LSI with very fine-pitch micro-joint, we noticed not only a continuous compressive stress distribution along the horizontal direction, but also a deep cross-sectional distribution of compressive stress. From this study, we qualitatively noticed that the residual mechanical stress/strain increases with the size of the micro-bump, i.e. it is higher for the larger bump size (as high as +240/-110 MPa) and lower for the smaller bump size (a maximum of +150/-70 MPa)

4. Conclusion

In the flip-chip bonded 3D-LSI die/wafer via metal micro bump, the metallic micro-joint exerted a large compressive stress for the region underneath the micro-bump, and it is extended up to more than 10 μm. Since this value is pretty close to the depletion region thickness, and for extremely thin LSI die/wafer it would have an adverse impact on the device characteristics.

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References

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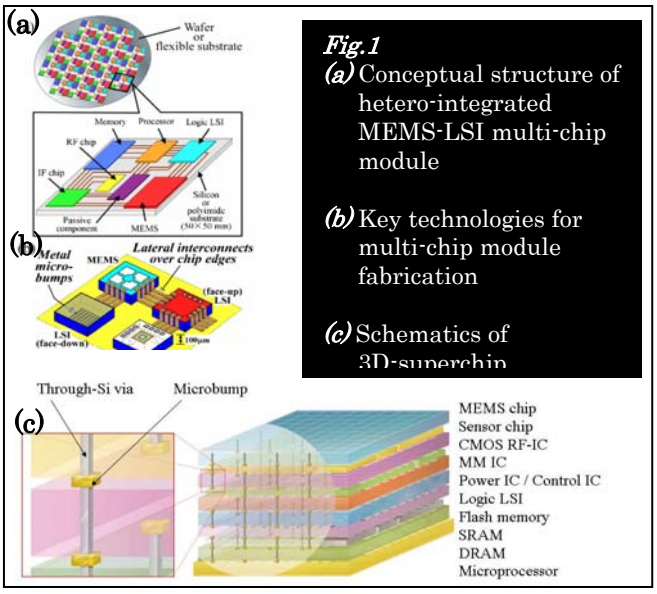

Fig.1
(a) Conceptual structure of hetero-integrated MEMS-LSI multi-chip module

(b) Key technologies for multi-chip module fabrication

(c) Schematics of 3D-superchip

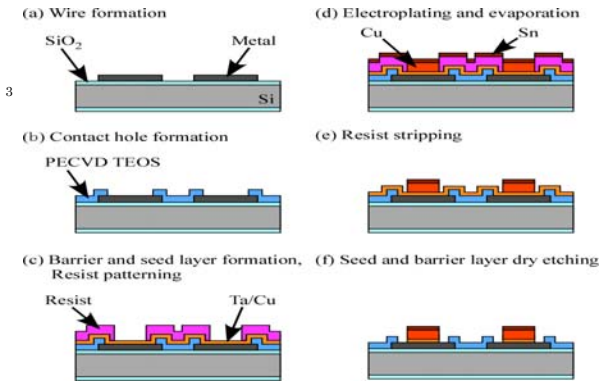

Fig.2 Fabrication process of Cu-Sn micro-bump formation

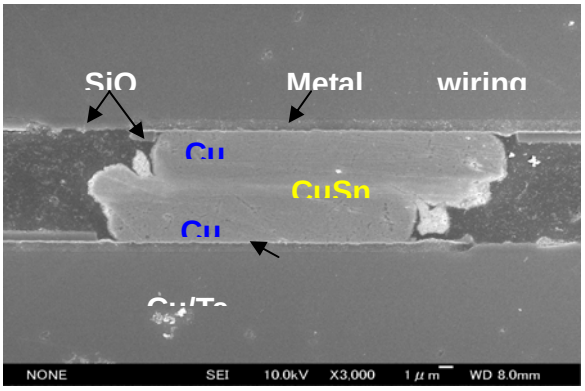

Fig. 3 Cross-sec. SEM view of Cu-Sn micro-joint.

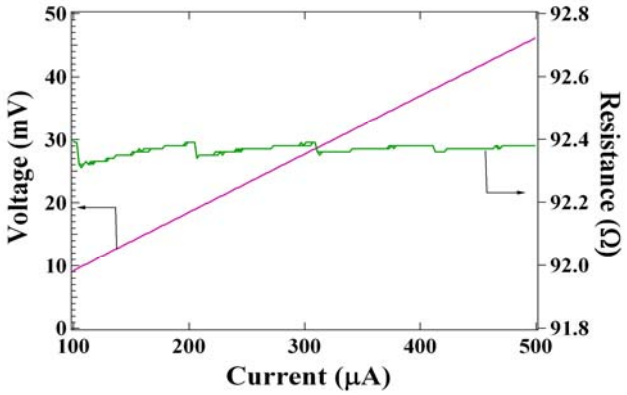

Fig. 4 I-V characteristics of the daisy chain consisting of 20 μm square, 40 μm pitch and 2500 CuSn micro bumps

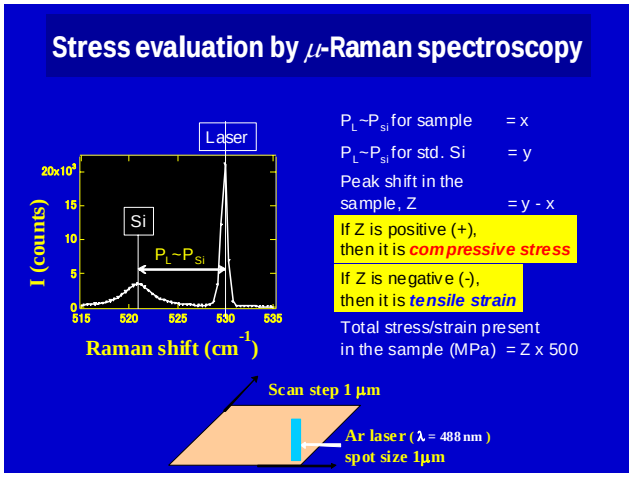

Fig. 5 Stress calculation from Raman data

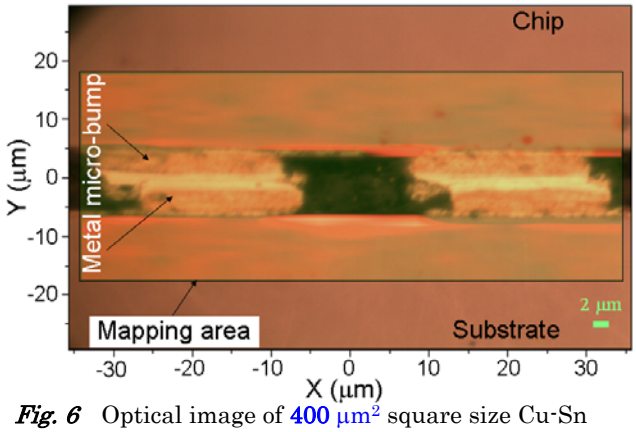

Fig. 6 Optical image of 400 μm² square size Cu-Sn micro-bump bonded LSI die/wafer. 2D-μR spectra were collected over the emboldened area.

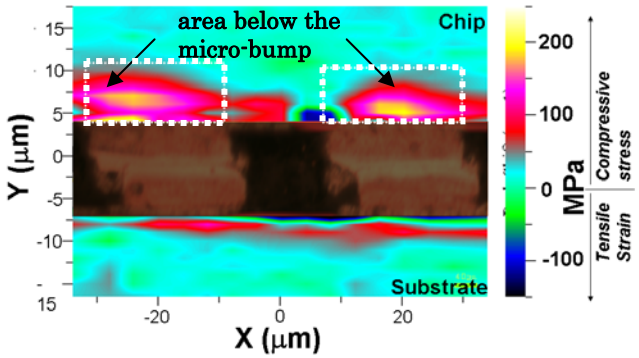

Fig. 7 Stress/strain distribution induced on the LSI die/wafer by 400 μm² square size Cu-Sn micro-bump.

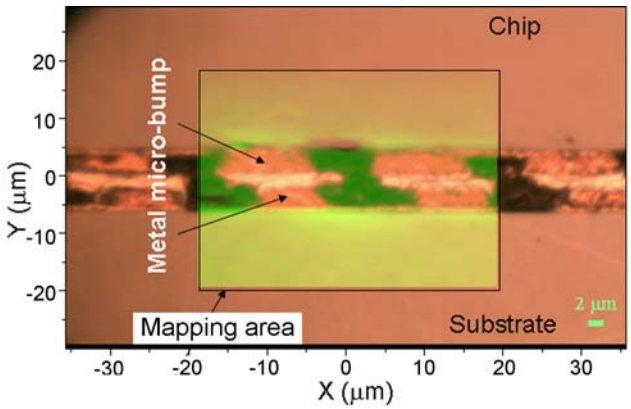

Fig. 8 Optical image of 100 μm² square size Cu-Sn micro-bump bonded LSI die/wafer. 2D-μR spectra were collected over the emboldened area.

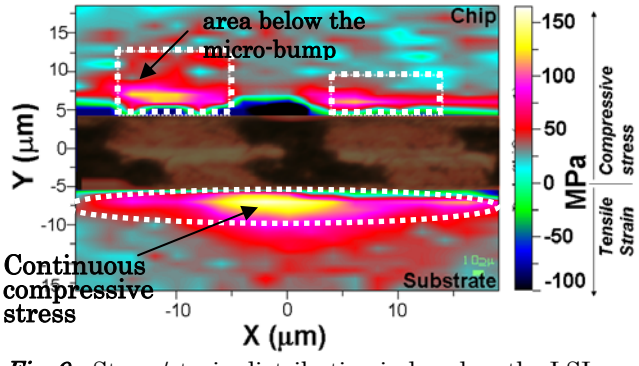

Fig. 9 Stress/strain distribution induced on the LSI die/wafer by 100 μm² square size Cu-Sn micro-bump.