

## High Density and Power Efficient SiP with SCS Technology

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### 1. Introduction

High bandwidth is required between logic and memory in recent System-on-Chip (SoC) devices to achieve high performance data processing. In addition, low power solution is also demanded, especially for mobile devices. One of the solution is embedded DRAM (eDRAM). eDRAM technology has been broadly used for several technology nodes. However, it faces some challenges after 90 nm technology node.

Stacked-chip SoC (SCS) is another solution as an alternative of SoC and have potential to overcome some challenges that eDRAM is facing. In this article, eDRAM and SiP are compared and region in which SiP shows better performance than eDRAM will be described.

### 2. Challenges for eDRAM Technology

#### 2.1 Slow Down of DRAM Cell Shrink Rate

eDRAM has been used for several technology nodes. DRAM cell size is reduced as progress of Si process as shown in Fig.1. eDRAM and logic devices were integrated based on DRAM technology at the beginning, but compatibility with logic device technology has been considered in process integration since 180 nm generation. As a result, shrinkage rate of DRAM cell is decreasing.

There are two kinds of DRAM cell, trench cell and stack cell. DRAM cell structure of trench type is shown in Fig. 2. In this structure, deep trench is formed in Si substrate and sidewall of the trench is used for capacitor. Aspect ratio and characteristics of dielectric material dominate the characteristics of DRAM cell. DRAM cell is formed before formation of MOS transistors in this structure, so trench cell structure has high compatibility with logic process. However, it is difficult to form deep trench with high aspect ratio, and there is limitation of selection of dielectric material. Due to the reasons, shrinkage rate of DRAM cell beyond 65 nm have to be reduced.

#### 2.2 Difficulty to Keep Reliability

Stack type of DRAM cell is the structure in which capacitors are made on MOS transistors, as shown in Fig. 3. Dielectric constant of dielectric material used for the capacitor determines characteristic and performance of DRAM cell. As Si technology node is progressed, dielectric ma-

terial with higher dielectric constant is used for DRAM cell. Since it is necessary to form capacitors on the wafer that MOS transistors are already formed, process temperature to form dielectric material needs to be lowered. It is difficult to improve quality of dielectric film in capacitors, and there are concerns about leakage and reliability.

### 3. Benefit of SiP with SCS Technology

#### 3.1 Structure of SiP with SCS Technology

Stacked-chip SoC (SCS) is a solution of high bandwidth connection between high performance logic and memory devices. Chip-on-chip (CoC) technology is used for SCS, and logic and memory devices are connected with high pin count. Fig. 4 shows the example of the structure of system-in-a-package (SiP) structure with SCS technology. Bump electrodes are formed on both logic and memory devices, and these are connected face to face each other. 40  $\mu\text{m}$  pitch bump electrodes is available now for mass production. In this case, bump area for 1 kbits connection is only 1.6  $\text{mm}^2$ . Fig. 5 shows cross section image of bump connection in SCS. Sn-Cu solder is used for bump electrode.

#### 3.2 Reliability Benefit of SiP with CoC Technology

Independent logic and memory devices are used in SiP with SCS technology and both devices can be fabricated with different manufacturing processes. Thus, compatibility of logic and DRMA process is not necessary, and reliability of DRAM device can be much improved by using suitable process for DRAM.

#### 3.3 Cost Benefit of SiP with CoC Technology

Fig. 6 shows cost comparison of eDRAM and SCS for several technology nodes. Two cases in which area of logic and memory are different are studied. In 65 nm generation, eDRAM shows advantage to SCS, but it is found that SCS shows relatively lower cost than eDRAM beyond 40 nm generation. Fig. 7 shows cost comparison for different memory capacity in 65 nm generation. SCS shows cost benefit if memory size is large.

#### 3.4 Power Consumption of SCS Technology

SCS has advantage in reliability and cost to eDRAM.

However power consumption has to be increased because additional I/O power is required.

Fig. 8 shows comparison of power consumption between SCS and conventional SiP with wire bonding. Active power of SCS is 1/12 of conventional SiP to achieve same bandwidth. High pin count connection is available in SCS and it is possible to reduce data transmission rate per pin and input capacitance.

Fig. 9 shows an example of SiP with SCS technology. In this case, 13 Si dies are integrated in a package. Footprint can be much reduced compared to external memories, and it helps to achieve miniaturization and cost reduction of system.

#### 4. Conclusion

It is necessary to select most suitable solution according to the requirement of the product. SCS technology is more reliable than eDRAM and realizes lower cost solution beyond 40 nm generation.

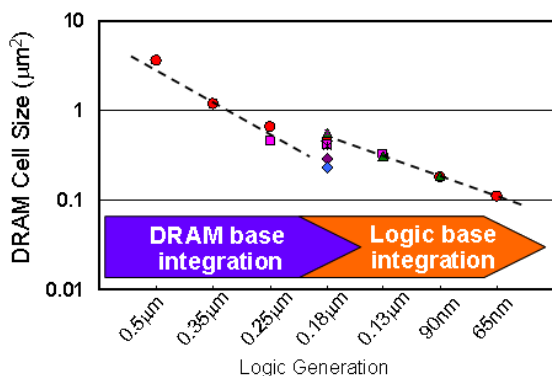


Fig. 1 Cell size of eDRAM in several technology nodes

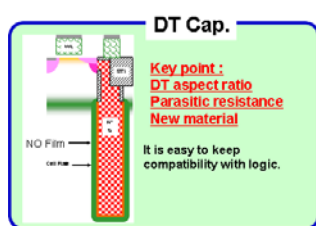


Fig. 2 Structure of trench DRAM cell

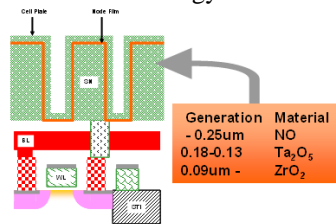


Fig. 3 Structure of stack DRAM cell

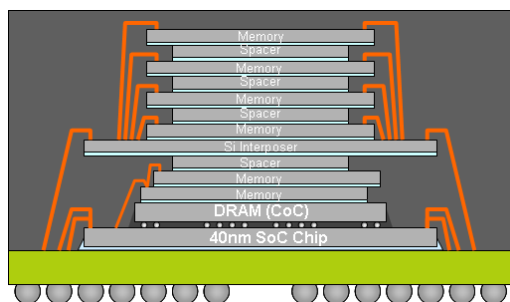


Fig. 4 Structure of SiP with CoC Technology

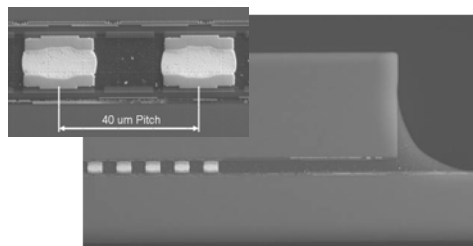


Fig. 5 Cross Section of Connection of Logic and Memory Dies with CoC Technology

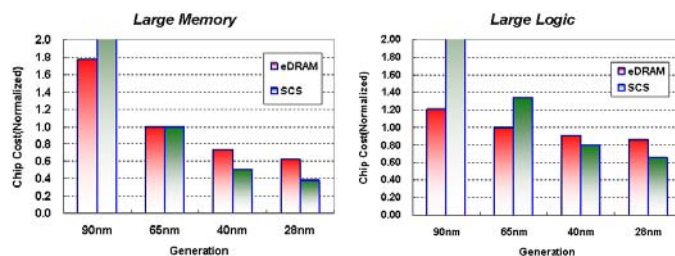


Fig. 6 Cost Comparison of eDRAM and CoC in several Si technology nodes

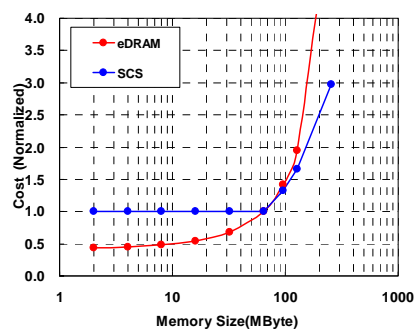


Fig. 7 Cost comparison between eDRAM and CoC technology for different memory size

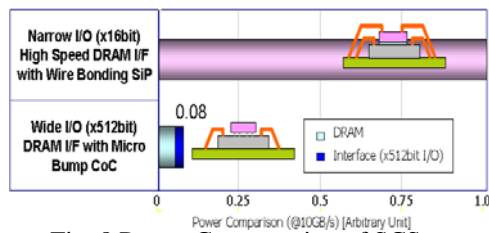


Fig. 8 Power Consumption of SCS

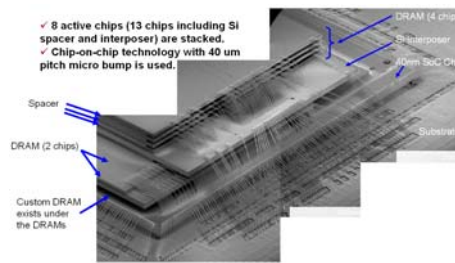


Fig. 9 SiP with SCS Technology

#### References

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