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Near-Infrared Image Sensor Fabricated Using Compliant Bump

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1. Introduction

Heterogeneous three-dimensional (3D) chip stacking [1,2], which involves stacking different types of chips (Si, II-VI/III-V compound semiconductor devices, MEMS devices, biosensors, etc.), is attracting considerable attention in the development of electronic systems with novel functionalities. For the successful implementation of this technology, heterogeneous chips must be bonded firmly without mechanical damage caused by the mismatch of the material constants (thermal expansion coefficient, hardness, etc.). Furthermore, the inclusion of an array of circuit elements, such as image sensors, in the stacked chip requires reliable high-density inter-chip connections.

To satisfy the above mentioned requirements, we have proposed the use of compliant bumps [3,4] such as Au cone bumps to achieve optimum chip stacking. Since these bumps can be easily deformed under compression, their use provides the following benefits (Fig. 1); (1) suppression of bonding failure, (2) reducing strain generation at the device level, (3) reliable bonding at low temperature, and (4) resin exclusion in the case of chip stacking with a precoated-resin. In the previous study, we used a compliant bump for homogeneous 3D stacking of Si chips and developed a back-side illuminated CMOS image sensor [5].

In this study, we apply a compliant bump to heterogeneous 3D chip stacking and demonstrate a near-infrared image sensor in which the compliant bump connects an InGaAs/InP photodiode chip to a CMOS read-out circuit chip at the pixel level.

2. Fabrication process

Figure 2 shows the fabrication process of the a near-infrared image sensor using compliant bump. In this study, Au cone bumps were prepared as compliant bumps, because hardness of Au is lower than that of InP and Si. First, Au cone bumps were formed on a CMOS read-out circuit wafer by formation of seed layer, photolithography (formation of undercut holes), Au electroplating, removal of resist, removal of seed layer and annealing [Fig. 2(a)]. Then, the InGaAs/InP photodiode wafer was thinned down to 320 μm by grinding, and an SiON film was deposited as an anti-reflection coating [Fig. 2(b)]. The back-side electrode was then formed for interconnection to the n-type region of the photodiode [Fig. 2(c)]. Both wafers were then diced. After Ar plasma cleaning, the Au/Ti electrodes on the InGaAs/InP photodiode chip were bonded to the Au cone bumps on the CMOS read-out circuit chip using the conventional flip-chip bonder [Fig. 2(d)]. The bonding conditions were as follows: pressing load was 0.75 gf/bump, bonding temperature was 300 °C, bonding time was 40 s, and atmosphere was air.

Figure 3 shows optical micrographs of the CMOS read-out circuit chip and the InGaAs/InP photodiode chip. The CMOS read-out circuit chip contains Au cone bumps (top size: 3–4 μm, base size: 12–13 μm, height: 7–8 μm), and the InGaAs/InP photodiode chip contains Au/Ti electrodes (base size: 13–14 μm). The number of active pixels was 76,800 (240 $\times$ 320) and the pixel pitch was 30 μm.

Figure 4 shows an optical micrograph of the near-infrared image sensor. We find that the InGaAs/InP photodiode chip is stacked onto to the CMOS read-out circuit chip by Au cone bumps.

3. Characteristics

Figure 5 shows the relative responsivity of the InGaAs/InP photodiode under back-side illumination. The maximum relative responsivity was observed at wavelength of 1320–1550 nm.

Figure 6 shows an example of image frames obtained by using the near-infrared image sensor. We find that a near-infrared image is obtained. This result demonstrates that the Au cone bump are useful for heterogeneous 3D chip stacking with high-density inter-chip connections. Although there were some defects, pixel operability of the image sensor was as high as 99.2% (76,174/76,800). The defects can be primarily attributed to the presence of some particles on both chips and can be reduced by removing the particles.

4. Conclusion

We demonstrated a near-infrared image sensor in which an InGaAs/InP photodiode chip was electrically connected to a CMOS read-out circuit chip through compliant bumps. The pixel operability of the sensor was 99.2% (76,174/76,800). The pixel pitch was 30 μm. An increase in the number of active pixels and a decrease in the pixel pitch can be easily realized by shrinking the Au cone bumps. Furthermore, room temperature bonding using the mechanical caulking effect of compliant bump [6] will facilitate the development of novel systems by integrating non-heat-resistant chips.

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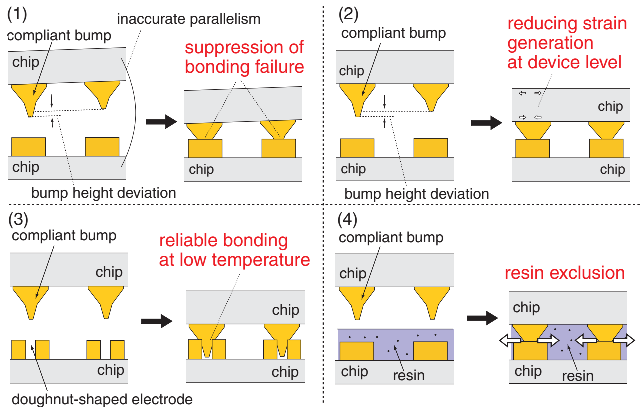

Fig. 1: Advantages of the compliant bump.

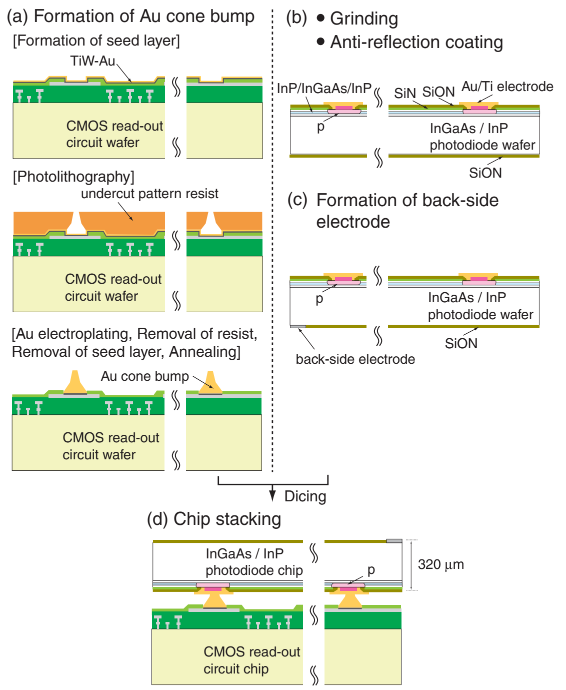

Fig. 2: Process flow of the near-infrared image sensor.

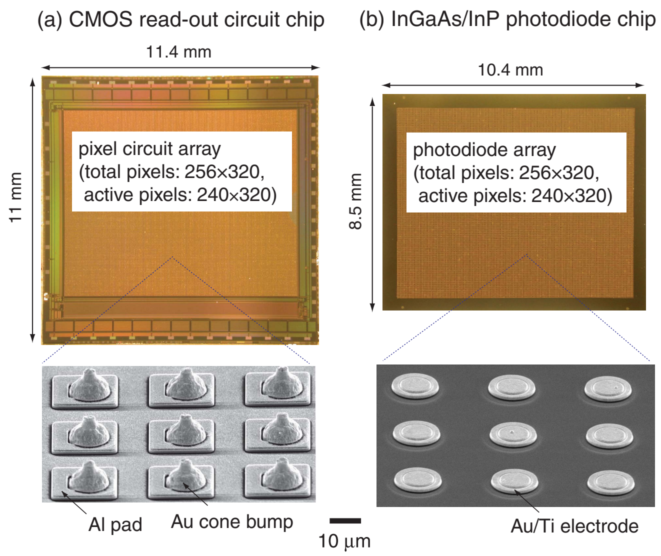

Fig. 3: Optical micrographs of the CMOS read-out circuit chip and the InGaAs/InP photodiode chip.

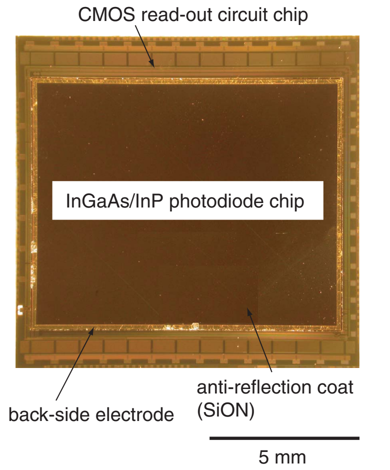

Fig. 4: Optical micrograph of the near-infrared image sensor. The InGaAs/InP photodiode chip is stacked onto the CMOS read-out circuit chip by Au cone bumps.

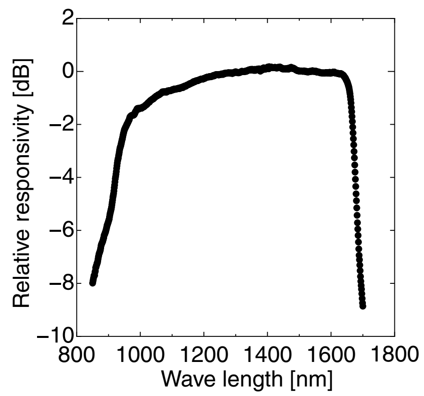

Fig. 5: Relative responsivity of the InGaAs/InP photodiode. The maximum relative responsivity was observed at wavelength of 1320–1550 nm.

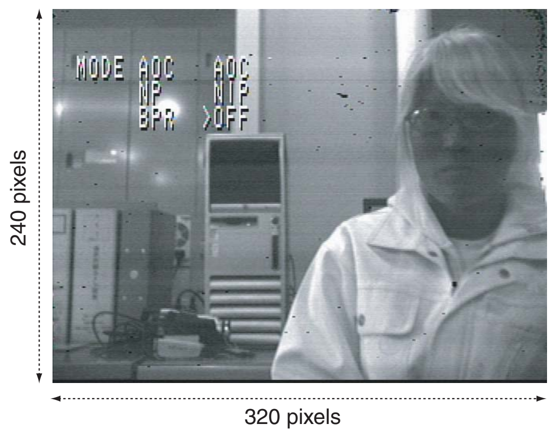

Fig. 6: Example of image frames obtained using the near-infrared image sensor. The pixel operability of the image sensor was 99.2%. (number of normal pixels = 76,174, number of defects = 626). No cooling was applied.