Adding Value to CMOS through Heterogeneous Integration

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Abstract
For the first time, technology capable of wafer-scale device-level integration of InP HBTs and CMOS has been developed. With this technology full simultaneous utilization of III-V device speed and CMOS circuit complexity is possible. Simple ICs and test structures have been fabricated, showing no significant CMOS or HBT degradation and high heterogeneous interconnect yield. Resulting circuits maintain maximum CMOS integration density and HBT performance, while keeping the heterogeneous interconnect length below 5 μm.

INTRODUCTION

III-V compound semiconductor device performance still greatly surpasses that of their Si counterparts, but CMOS has orders of magnitude higher level of integration. Device-level integration of CS devices with CMOS would enable a new class of high-performance high-functionality ICs [1] at a cost similar to CS ICs alone. For such heterogeneous ICs, InP DHBT technology is particularly suited due to the high device performance [2], high IC speed at low power [3], and circuit compactness. In this work we present first demonstration of wafer-scale device-level heterogeneous integration (HI) of 250nm, 300GHz fT/fMAX InP DHBT technology with IBM’s 130nm RF-CMOS (CMRF8SF) technology.

PROCESS TECHNOLOGY

For this technology, InP DHBT epitaxial layers are bonded to the top interconnect layer of a CMOS wafer, which are then processed into HBTs and interconnected with the CMOS. This process is illustrated in Figure 1. The CMOS interconnect process is terminated at the last planar interconnect layer to enable epitaxial transfer, with only a thin dielectric layer on top of the copper. The 200mm CMOS wafers are then cut into four 3inch wafers so that they can be further processed in our HBT line. Standard DHBT epitaxial layers are grown on InP substrate with thin etch stop layers inserted right above the substrate. The DHBT wafer is then wafer bonded to a temporary Si handle wafer. The growth InP substrate is removed by wet etching, stopping on the etch stop layers. The DHBT wafer is then wafer bonded to a temporary Si handle wafer. The growth InP substrate is removed by wet etching, stopping on the etch stop layers. An Al heat spreader layer is deposited on the subcollector. The epitaxial layers are then permanently bonded to the top CMOS surface using BCB adhesive layer [4]. After the permanent bonding, the handle is removed, completing the epitaxial transfer process. The CMOS wafer contains the alignment marks needed for the HBT processing. InP DHBT fabrication process on top of CMOS is similar to the standard process [5]. Alignment accuracy to the CMOS and between the HBT layers is equal to our standard HBT process. Despite increased overall topography, critical dimension control for both electron beam and optical lithography is maintained. After the HBT is fabricated, the heat spreader and the adhesion layers are patterned. The HBT and CMOS are finally interconnected through HI vias. In addition to electrical vias, thermal vias that connect the heat spreader to the Si substrate are also fabricated. Only one post-CMOS interconnection layer is used. All other interconnect layers as well as resistors and capacitors are done in the CMOS interconnect layers.

RESULTS

Using the above technology, differential amplifier ICs [6] and DC and RF test structures were fabricated. The ICs demonstrated gain bandwidth product of 40-130 GHz and low frequency gain >45dB. The use of InP DHBTs supports a 6.9 V differential output swing and a slew rate >4x10^4 V/μs, achieved with as low as 40mW dissipated power. Presence of CMOS enabled the use of novel on-chip buffer circuits to facilitate the on-wafer characterization of these amplifiers. For the CMOS test devices, the IV characteristics of various IBM CMRF8SF library devices from HRL
fabricated heterogeneously integrated wafers showed no signs of device degradation when compared to control IBM CMOS wafers. Figure 2 shows the typical transfer characteristics of a 1.5V thin-oxide, triple-well NFET (LG=120nm, WG=5.0μm) bias at a VDS=1.5V and VBS=0.0V. A sparse sampling of 10 devices from a single HI wafer (left) and 22 devices from a quarter of the IBM control CMOS wafer (right) are shown.

Characteristics of a 1.5V thin-oxide, triple well NFET sampled from an HRL fabricated HI wafer and an IBM fabricated control CMOS wafer. The HI HBTs performance was on par with our standard HBTs. For an A_{E}=0.25x4.0μm^{2} InP DHBT, Figure 3 (left) shows the forward Gummel characteristics and a DC current gain (β_{f}) >30; Figure 3 (right) shows common emitter IV characteristics and low output conductance; and Figure 4 shows f_{T} of 400GHz and modest f_{MAX} of 244GHz. Peak f_{MAX} is limited by a higher R_{B} and C_{BC} resulting from the starting epitaxial material and the additional parasitic loading of the thermal via. In order to assess the yield and resistive loss of the HI via, a 1000 unit long chain of the nominal 1.0x1.0μm^{2} HI vias at a pitch of 5μm were electrically tested. Figure 5 shows the average HI via resistance is <400mΩ across the majority of the 3inch diameter wafer.

CONCLUSIONS

Novel wafer-scale device-level heterogeneous integration technology is demonstrated. Dense HI integration without device degradation enables ICs that maintain both CS performance and CMOS functionality. This technology is applicable to any generation CMOS and HBTs, as well as other CS devices. CS device integration with CMOS could accelerate its maturity and utilization.

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