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InP/InGaAs MOSFET with Back-Electrode Structure Bonded on Si Substrate Using a BCB Adhesive Layer

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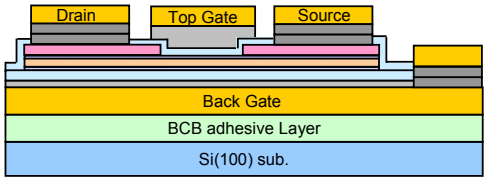
1. Introduction

According to ITRS 2009, the drain current of MOSFET for high-performance logic circuits will reach around 2 A/mm after 2020 [1]. One way to achieve that requirement is to introduce high-mobility channel materials. III-V compound semiconductors such as InGaAs can potentially be introduced into LSI as n-channel materials because of their small electron effective mass and high mobility. Logic applications using III-V devices have already been studied. Conventional InP-based transistors with HEMT device structures have been fabricated [2]. Furthermore, III-V MOSFETs with high-k dielectrics have been studied [3]−[7]. Previously, we have reported III-V MOSFET operation on InP substrates [8]. However, to achieve Si integration and high-current operation, a device-layer transfer to Si and a backside fabrication process are desirable.

In this report, we demonstrate planar-type MOSFET with an InP/InGaAs/InP composite channel and a back-gate structure formed by wafer bonding on Si (100) substrate using a benzocyclobutene (BCB) adhesive layer.

2. Device Structure and Fabrication Process

A schematic image and the layer profiles of the DGFET fabricated in this study are shown in Fig. 1.



(a) Schematic image

Top Gate	Source/Drain	grown sub. (upside down)	Thickness	roles
	Au 160 nm	p-InP sub.	600 μm	substrate
Au 160 nm	Pd 20 nm	InGaAs	200 nm	etch stop
Cr 40 nm	Ti 20 nm	InP	10 nm	etch stop
Al_2O_3 10 nm	n⁺-InGaAs	n⁺-InGaAs	72 nm	contact
InP	InP	InP	5 nm	channel
InGaAs	InGaAs	InGaAs	12 nm	channel
InP	InP	InP	5 nm	channel
Al_2O_3 15 nm		InGaAs	20 nm	cap
Cr 10 nm		InP	20 nm	cap
Au 160 nm		-	-	-
BCB adhesive layer		-	-	-
Si (100) sub.		-	-	-

(b) Layer profiles of device and substrate

Fig. 1 Schematic device structure and layer profiles

We used 5-nm-thick InP/12-nm-thick $In_{0.53}Ga_{0.47}As$/5-nm-thick InP undoped composite channel structure to separate the electrons from a channel/dielectric interface to reduce the carrier scattering caused by roughness and trap charges. Non-alloy source/drain contact was formed by heavily doped ($\approx 5 \times 10^{19}$ cm^{-3}) InGaAs and Ti/Pd/Au contact metals. Back-gate stack existed below the channel and a source/drain and back-gate contact pad was fabricated on the upside. The length and width of the channel were 2 μm and 20 μm, respectively. The top/back-gate dielectrics were Al_2O_3. The thickness of the Al_2O_3 was 10 nm as a top-gate and 15 nm as a back-gate and these EOT were estimated about 4.5 nm and 6.8 nm, respectively ($\varepsilon_r \approx 8.6\varepsilon_0$). The device layers were grown on p-type InP substrate using metal organic vapor phase epitaxy (MOVPE). The 72-nm-thick n$^+$-InGaAs contact layer was grown under the channel for the bonding process.

The fabrication process was as follows. First, the InP/InGaAs cap layers on the 5-nm-thick InP channel layer were removed by wet etching. An Al_2O_3 gate dielectric was deposited by atomic layer deposition after surface passivation using $(NH_4)_2S$ for 10 min. A Cr 10 nm/Au 160 nm back-gate electrode was then deposited by electron beam evaporation. Next, the Si(100) substrate was cleaned using sulfuric peroxide mixture solution (H_2SO_4:H_2O_2 = 4:1) and SC1 solution (NH_4OH:H_2O_2:H_2O = 1:4:25). BCB was then spin coated on the Si substrate with surface activation and pre-curing was done in an N_2 oven at 50°C for 1 h. Next, the sample was bonded on the Si substrate coated by BCB with a bonding pressure of 12 N and a temperature of 130°C in a vacuum. After the heat bonding, the sample was baked at 250°C in an N_2 oven for 1 h. Then, the InP substrate was fully etched by HCl and the InGaAs/InP etch stop layers were also wet etched. The device layers were then isolated by wet etching to Al_2O_3 using citric acid:H_2O_2 = 1:1 and HCl:H_2O = 3:1. Next, contact n$^+$-InGaAs on the intrinsic channel region was etched to the InP surface using a citric-acid solution. 10-nm-thick top-gate dielectric was deposited using a similar process to that at the back-gate and a Cr/Au electrode was formed. Then, post-metallization rapid thermal annealing was carried out in N_2 ambient at 350°C for 90 s. Finally, contact holes to the source/drain and back gate were formed by BHF etching of Al_2O_3 and Ti/Pd/Au was evaporated. A cross-sectional SEM image of the source region is shown in Fig. 2

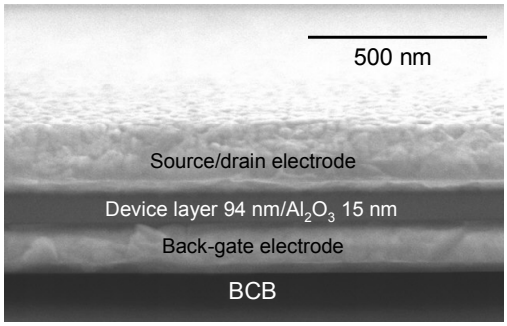
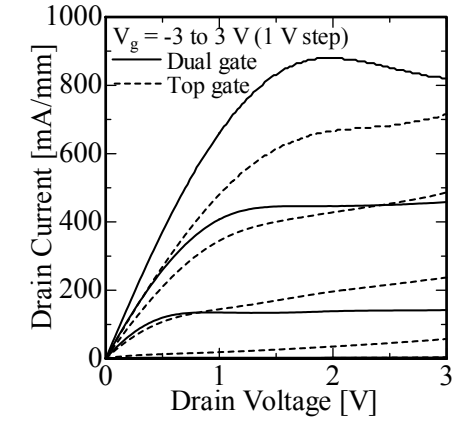


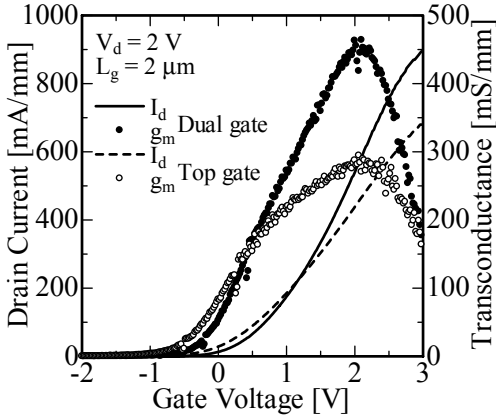
Fig. 2 Cross sectional SEM image of bonding structure

3. I-V Characteristics

Figure 3 shows the I-V characteristics of MOSFET with only top-gate bias (V_{tg}) operation (the back-gate was floated) and dual-gate operation (V_{tg} = back-gate bias (V_{bg})).



(a) I_d-V_d characteristics



(b) I_d-V_g characteristics

Fig. 3 I-V characteristics of fabricated MOSFET

The maximum drain current (I_d) at $V_{tg} = V_{bg} = 3$ V and the drain voltage (V_d) of 2 V was 880 mA/mm and the peak transconductance (g_m) was 450 mS/mm at $V_d = 2$ V in the dual-gate measurement. These values were higher than those for single-gate operation which had a similar performance to non-bonded devices: $I_d = 715$ mA/mm and $g_m = 280$ mS/mm. In particular, a clear enhancement in the g_m characteristics was achieved. A negative drain conductance was observed in the saturation region at high gate voltagea (> 2 V). The on/off ratio of the MOSFETs was above 10^6 at $V_d = 2$ V.

The threshold voltage of the dual-gate mode operation shifted to positive compared with single-gate mode operation and enhancement mode operation was nearly obtained. From the resistance dependence on the channel length, the total series resistance was 0.75 Ω·mm and the sheet resistance was 373 Ω/square. The subthreshold slope was around 300 mV/dec and the drain-induced barrier lowering at $I_d = 0.1$ mA/mm was 296 mV/V. These values were not improved by the dual-gate operation; they might be restricted by the characteristics of the high-k/channel interface and the channel thickness.

4. Conclusion

We have reported InP/InGaAs/InP composite channel MOSFET with a Cr/Au back-gate structure on Si substrate using the BCB bonding process. In the I-V measurement of fabricated MOSFET with dual-gate operation mode, the maximum drain current at $V_{tg} = V_{bg} = 3$ V, $V_d = 2$ V was 880 mA/mm and the peak transconductance at $V_d = 2$ V was 450 mS/mm. The peak transconductance was 50% larger than that of only top-gate modulation alone. These results demonstrate the capability of Si integration and the backside fabrication process of thin-body III-V materials such as multi gate or field effect accumulation in the source backside.

Acknowledgements

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