Extended Abstracts of the 2010 International Conference on Solid State Devices and Materials, Tokyo, 2010, pp131-132

Source/Drain Engineering for $In_{0.7}Ga_{0.3}As$ N-MOSFETs: Raised Source/Drain with *In Situ* Doping for Series Resistance Reduction

Xiao Gong,[1,2] Hock-Chun Chin,[1] Shao-Ming Koh,[1] Lanxiang Wang,[1,2] Ivana,[1,2] Zhu Zhu,[1]
Benzhong Wang,[3] Ching Kean Chia,[3] and Yee-Chia Yeo.[1,2,*]

[1] Dept. of Electrical & Computer Engineering, National University of Singapore, 117576 Singapore.
[2] NUS Graduate School of Integrative Sciences and Engineering, National University of Singapore, 117456 Singapore.
[3] Institute of Materials Research and Engineering, Agency for Science Technology and Research, 117602 Singapore.
[*] Phone: +65-6516-2298, Fax: +65-6779-1103, Email: yeo@ieee.org

ABSTRACT

We report the first demonstration of $In_{0.7}Ga_{0.3}As$ N-MOSFETs with *in situ* doped raised source/drain (S/D) regions. The raised S/D structures were fabricated by selective MOCVD grown of InGaAs layer after SiN spacer formation. *In situ* SiH_4 doping was also introduced to boost the N-type doping concentration. By using the new S/D architecture, a ~30% reduction in series resistance R_S can be obtained, leading to enhancement in I_{Dsat} of the $In_{0.7}Ga_{0.3}As$ N-MOSFETs.

INTRODUCTION

High mobility III-V compound semiconductors are attractive candidates to replace strained Si channel for future high performance logic applications [1]-[4]. Recent research on III-V MOSFETs has focused on gate stack and interface engineering, with very promising results obtained [5]-[8]. To harness the full potential of III-V MOSFETs, S/D engineering is an important direction. $In_{0.53}Ga_{0.47}As$ channel N-MOSFETs with *in situ* doped S/D [2] and GaAs FETs with the first self-aligned metallization technology for III-V MOSFETs were recently demonstrated [9]. Significant reduction in series resistance was achieved.

In this paper, we report the demonstration of raised S/D structures with *in situ* doping for $In_{0.7}Ga_{0.3}As$ N-MOSFET. Significant series resistance reduction and drive current improvement were demonstrated.

DEVICE DESIGN AND FABRICATION

The process flow for device fabrication is illustrated in Fig. 1. The cross-sectional TEM image in Fig. 2(a) shows a completed $In_{0.7}Ga_{0.3}As$ channel N-MOSFET with the raised $In_{0.53}Ga_{0.47}As$ S/D structures, and the high-resolution TEM image in Fig. 2(b) confirms the pseudomorphic epitaxial growth of $In_{0.53}Ga_{0.47}As$ on $In_{0.7}Ga_{0.3}As$. Fast Fourier transform (FFT) diffractogram reveals good crystalline quality of $In_{0.53}Ga_{0.47}As$ epilayer.

500 nm $In_{0.55}Ga_{0.45}As$ well with P-type doping concentration N_A of 5×10^{17} cm^{-3} and 20 nm $In_{0.7}Ga_{0.3}As$ channel with lower N_A of 1×10^{16} cm^{-3} were sequentially grown on InP substrate. HRXRD in Fig. 3 confirms the composition and high crystal quality of the InGaAs epilayers. After pre-gate cleaning in HCl, NH_4OH, and $(NH_4)_2S$, the samples were quickly loaded into a multiple-chamber MOCVD gate cluster system for interface engineering and HfAlO deposition [10]. Post-gate dielectric deposition anneal (PDA) at 500 ℃ for 60 s were performed prior reactive sputter deposition of TaN. 70 nm of PECVD SiO_2 was also deposited to cover the top surface of TaN gate electrode for selective epitaxy. After gate definition, S/D regions were formed after implantation and dopant activation. SiON spacer was also integrated to cover the side wall of the gate stack for subsequent selective MOCVD epitaxy process to form the raised S/D structures.

The MOCVD process was conducted at 635 ℃ and chamber pressure of 75 Torr. Trimethylgallium (TMGa), tertiarybutylarsine (TBA), and trimethylindium (TMIn) were employed as the precursors. Flow rates for TMGa, TBA and TMIn were 16 sccm, 60 sccm and 130 sccm, respectively. SiH_4 was used to achieve *in situ* N-type doping of 5×10^{19} cm^{-3}. The MOCVD process was skipped in the control devices. Finally, PdGe ohmic contacts were integrated to complete the device fabrication.

RESULTS AND DISCUSSION

Identical EOT of 6.8 nm was found in both devices, as shown in inversion *C-V* characteristics (Fig. 4). Fig. 5 plots the I_D-V_G curves of both $In_{0.7}Ga_{0.3}As$ transistors. I_D-V_D characteristics of the same pair of devices are shown in Fig. 6. Significant drive current enhancement was observed in the InGaAs device with new raised S/D structures. Fig. 7 shows the extrinsic transconductance $G_{m,ext}$ versus V_G for both N-MOSFETs. Considering this pair of devices, the raised S/D architecture with *in situ* doping gives rise to 28% enhancement in saturation $G_{m,ext}$.

The total resistance R_{Total} versus V_G curves in Fig. 8 examine the total resistance at high gate overdrive, at which the R_S dominates at low channel resistance. Using the extraction method proposed by [11], the R_S of raised S/D device and control were extracted to be 3.1 kΩ·μm and 3.9 kΩ·μm, respectively. Fig. 9 shows the cumulative distribution of series resistance. The statistical result shows ~30% reduction in the median R_S. I_{Dsat} enhancement of ~30% at a fixed I_{OFF} of 10^{-6} A/μm was achieved by using this new S/D engineering approach, as illustrated in Fig. 10. Fig. 11 benchmarks the normalized peak G_m of $In_{0.7}Ga_{0.3}As$ devices with *in situ* doped raised S/D structure in this work with our previous work [2]. G_m was normalized with C_{ox} to account for the difference in EOT. Higher normalized peak G_m was achieved here due to higher indium composition of 70% in the channel for improved electron mobility.

CONCLUSION

Raised S/D structure with *in situ* doping process was demonstrated for the first time in $In_{0.7}Ga_{0.3}As$ MOSFETs. Significant R_S reduction was achieved, leading to very substantial I_{Dsat} enhancement. This new S/D engineering approach is promising for R_S reduction in III-V MOSFETs.

Acknowledgement. This work is supported by National Research Foundation and Defence Science and Technology Agency, Singapore.

REFERENCES

[1] R. Chau *et al.*, *IEEE T. Nanotechnology* 4, pp. 153, 2005.
[2] H.-C. Chin *et al.*, *Symp. VLSI Tech. Dig.*, pp. 244, 2009.
[3] Y. Xuan *et al*., *IEDM Tech. Dig*, pp. 371, 2008.
[4] D.-H. Kim *et al.*, *IEDM Tech.. Dig.*, pp. 719, 2008.
[5] H.-C. Chin *et al*., *IEDM Tech. Dig*, pp. 383, 2008.
[6] J. Q. Lin *et al.*, *IEDM Tech. Dig*., pp. 401, 2008.
[7] H.-J. Oh *et al.*, *IEDM Tech. Dig*., pp. 339, 2009.
[8] Y. Q. Wu *et al.*, *IEDM Tech. Dig*., pp. 323, 2009.
[9] X.-G. Zhang *et al.*, Symp. *VLSI Tech*, 2010.
[10] H.-C. Chin *et al.*, *IEEE TED*, vol. 57, pp. 973, 2010.
[11] A. Dixit *et al.*, *IEEE TED*, vol. 52, pp. 1132, 2005.

- Pre-Gate Clean
- Interface Engineering and MOCVD HfAlO Deposition
- TaN and SiO_2 Hardmask Deposition
- Gate Definition
- S/D Implantation
- Splits:
  - *In-situ* Doped Raised S/D
    - Dopant Activation
    - SiON Spacer Formation
    - Selective Epitaxy of *In-situ* Doped $In_{0.53}Ga_{0.47}As$
  - Control
    - Dopant Activation
- PdGe Contact Formation

Fig. 1. Process sequence employed in the fabrication of $In_{0.7}Ga_{0.3}As$ channel N-MOSFETs with *in-situ* doped raised S/D.

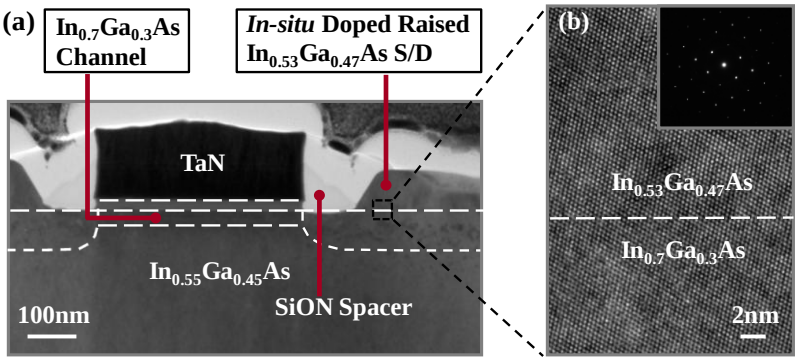

Fig. 2. (a) TEM image of a completed $In_{0.7}Ga_{0.3}As$ channel N-MOSFET with selectively grown *in-situ* doped raised S/D. (b) High resolution TEM and Fast Fourier transform (FFT) diffractogram, revealing the excellent crystalline quality of the $In_{0.53}Ga_{0.47}As$ epilayer.

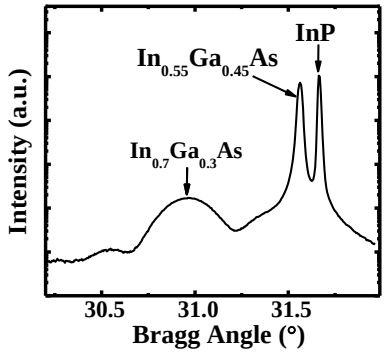

Fig. 3. HRXRD shows well-defined $In_{0.7}Ga_{0.3}As$ and $In_{0.55}Ga_{0.45}As$ peaks, indicating high crystalline quality of the epilayers.

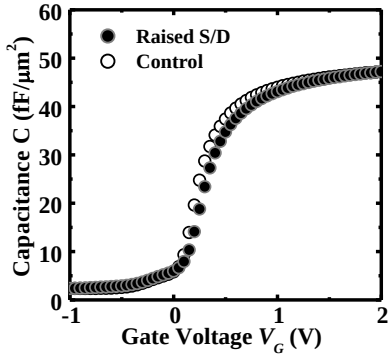

Fig. 4. Inversion C-*V* curves show comparable EOT of devices with raised S/D and control.

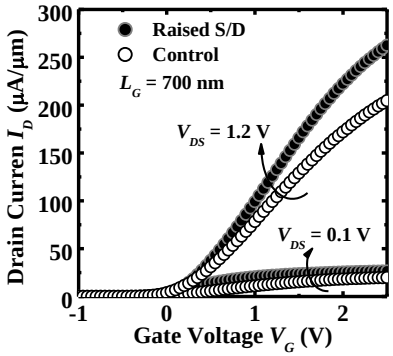

Fig. 5. I_D-V_G plots show I_D improvement in $In_{0.7}Ga_{0.3}As$ N-MOSFET with raised S/D.

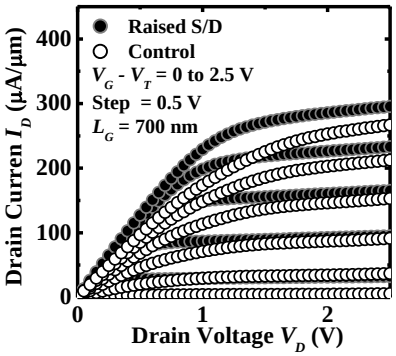

Fig. 6. I_D-V_D curves of same pair of devices in Fig. 5. Higher drive current was achieved for devices with raised S/D.

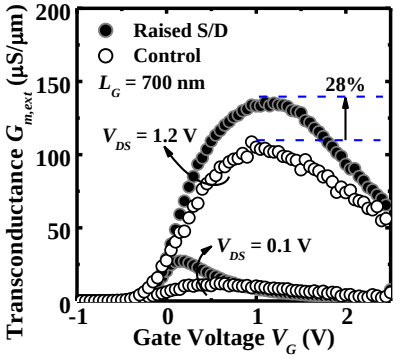

Fig. 7. $G_{m,ext}$-V_G curves of same pair of devices in Fig. 5. *In-situ* doped raised S/D gives rise to a 28% enhancement in saturation $G_{m,ext}$.

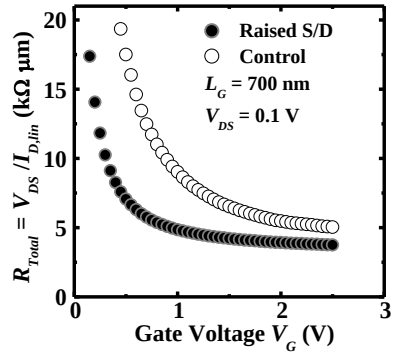

Fig. 8. Total resistance in linear regime at large V_G indicates smaller series resistance of devices with raised S/D than that of control.

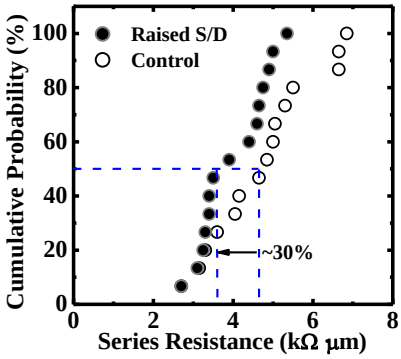

Fig. 9. *In-situ* doped raised S/D leads to ~30% series resistance reduction in the median.

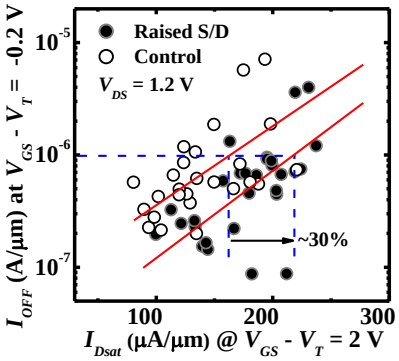

Fig. 10. *In-situ* doped raised S/D results in a ~30% enhancement of I_{Dsat} at a fixed I_{OFF} of 10^{-6} A/μm.

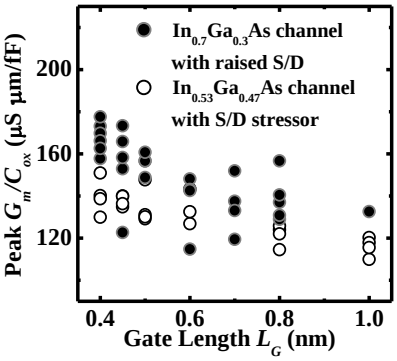

Fig. 11. Normalized peak G_m at V_{DS} = 1.2 V versus L_G. $In_{0.7}Ga_{0.3}As$ channel devices with raised S/D show higher normalized peak G_m.