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A sub 350ºC GaSb pMOSFET with ALD high-k dielectric

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Opportunity & Challenge: Sb based III-V semiconductors are one of the most promising device candidates for future high-speed, low-power logic applications. Some of the key strengths (Fig. 1) of Sb based semiconductors include: highest hole & electron mobility [1-2] among all III-V semiconductors, high conduction & valence band offsets (CBO/VBO) with lattice matched $Al_xGa_{1-x}Sb$ for a heterostructure MOSFET design [1] and low thermal budget for MOSFET fabrication (as discussed later). The challenges in implementation of Sb based channels for CMOS is the highly reactive Sb surface (Fig. 2). A high quality dielectric and a good diode is needed for realization of Sb-MOSFETs. In this paper we attempt to overcome these challenges and fabricate a GaSb pMOSFET. GaSb is selected as it has the highest hole mobility amongst all III-V's & has a bandgap of 0.72eV similar to Ge. pMOSFET was attempted first as it has been an impendent in implementation of III-V complimentary logic.

Introduction: In this paper Synchrotron Radiation Photoemission Spectroscopy (SRPES) is used to study the effect of various chemical cleans & subsequent anneal in UHV on GaSb to render a surface free of elemental oxide & suitable for dielectric deposition. Bandgap & offsets for ALD Al_2O_3 on GaSb are calculated using SRPES. Interface properties of the dielectric are investigated by analyzing the capacitance & conductance characteristics. A p^+/n diode on GaSb with $I_{ON}/I_{OFF} > 5\times10^4$ is developed. Finally, output characteristics on a gate-first self-aligned GaSb pMOSFET are presented.

Surface/SRPES analysis: Desorption of SbO_x and GaO_x on as received GaSb was studied by annealing under UHV till 400ºC. SbO_x starts to desorb at 400ºC and a Sb 4d peak from the substrate is observed, while GaO_x is found to be thermally stable and no desorption till 400ºC is observed (Fig. 3). Effectiveness of different chemical cleans on removing the GaO_x and SbO_x was studied low energy (hν=100eV) radiation from the synchrotron which allows observing the top few monolayers of the surface with great accuracy (Fig. 4). HF, HCl (acidic) and NH4OH (basic) cleans were tried. While all HF, HCl & NH4OH reduce GaO_x, only HCl based clean is able to effectively reduce SbO_x. A subsequent anneal after HCl clean reveals a GaSb surface free of native oxide (Fig. 5). Tapping mode AFM was used to study the surface, the RMS roughness just after HCl clean and after 10 cycles of ALD deposition were found to be 0.664 & 0.727nm respectively. Table. 1 compares the RMS roughness with Si/Ge. As SRPES has a high energy resolution at the valence band spectrum maximum, VBO can be precisely extracted by taking difference between spectrum before/after Al_2O_3 deposition (Fig. 6). VBO for Al_2O_3 on GaSb was determined to be 3.1eV, Sb 4d peak from the substrate was used for alignment [4]. The Bandgap was determined to be 6.3eV from the Al 2p loss spectrum (Fig. 7) [4] which agrees well with values reported in literature for Al_2O_3 deposited using ALD under similar conditions [5]. Taking the bandgap of GaSb (0.72eV) into account the band diagram was constructed as shown in Fig. 8. The CBO/VBO of 2.48eV/3.1eV for Al_2O_3 on GaSb is sufficient to minimize the electron/hole tunneling and is suitable for MOSFET fabrication.

Process Development: Two key steps in developing a process for GaSb were the dielectric development for the gate stack and the source/drain junction formation.

(a) Dielectric: Fig. 9 shows the CV characteristics on capacitors made on n-type & p-type substrate. 70 cycles of ALD Al_2O_3 were deposited at 300ºC & Pt was used as the gate electrode. Inversion response was observed on both n/p-type GaSb. Frequency dispersion in accumulation is ~2%/decade for p-type & ~5%/decade for n-type. Higher frequency dispersion under accumulation in n-type GaSb suggests a higher Dit near the conduction band edge. Dit is calculated applying the conductance method (Fig. 10) in depletion region [6]. Both n/p-type substrates substrate are used for conductance measurement and the temperature is varied from 300K-77K to probe the Dit distribution across the entire bandgap. A mid bandgap Dit of 3×10^{11} cm^{-2} eV^{-1} is obtained. The Dit distribution is asymmetric with an order of magnitude higher Dit towards the conduction band side, this is in qualitative agreement with the fact that CNL of GaSb is located at ~0.1eV from the valence band edge [7].

(b) Diode Development: Obtaining good diode characteristics in GaSb using ion implantation has been a problem traditionally, due to hillock formation because of implant damage [8]. Zn & Be which act as shallow acceptors in GaSb were tried for formation of p^+/n diode. Hillock formation was observed with Zn (dose $3\times10^{14}/cm^2$) which couldn't be removed by annealing in RTA. Only Be (being a lighter atom) implant was successful with high enough dose suitable for transistor fabrication. Fig. 11 shows the diode characteristics with various implant conditions. Sheet resistance decrease with anneal temperature saturates at 350ºC and good diode characteristics with I_{ON}/I_{OFF} of $>5\times10^4$ with ideality factor of 1.3 could be obtained with annealing at 350ºC for 30 min (Fig. 11). There is room for further improvement with more optimization of implant dose and energy.

Process flow: The low temperature required for S/D activation allows for a gate-first process flow. Fig. 12 summarizes the process flow : 100 cycles (~10nm) of ALD Al_2O_3 deposited at 300ºC was used as the gate dielectric followed by Al evaporation and gate patterning. S/D contacts were formed with Ti/Ni liftoff. Fabrication of the transistors was completed with a 350ºC FGA anneal which also activates the S/D implant. Maximum temperature during the entire process flow never exceeds 350ºC.

Transistor results: Fig. 13 plots the I_D-V_G for GaSb pMOSFET. I_{ON}/I_{OFF} of $> 10^3$ was obtained. Mobility vs. sheet charge in Fig. 14 is extracted on using I_D-V_G on the L_G=100µm device at V_{DS}=10mV & sheet charge is calculated from the C_{gc} measured at 100kHz. No corrections for S/D resistance are applied. Hole mobility in our device is comparable to silicon with similar doping density. Mobility in our device decreases with decrease in temperature (Fig. 14) indicating the mobility is not limited by phonon scattering mechanisms. Mobility in the high sheet range could be limited by the interface roughness which was measured to be 3-4 times higher in GaSb as compared to Si/Ge (Table. 1)

Summary: ALD Al_2O_3 gate stack & p^+/n diode are developed on GaSb. Peak inversion hole mobility of $85cm^2/Vs$ is the highest reported to date for GaSb pMOSFET.

[1]A. Nainani et. al., IEDM 2009 p. 857 [2]B.R. Bennett et. al., Solid State Electronics, 49, pp. 1875 [3] A. Nainani et. al., submitted SISPAD 10 [4] M. Kobayashi et. al. SSDM 08, p. 1056 [5] N.V. Nguyen et. al. 96 (5), 052107[6] E. H. Nicollean et. al., Bell Syst. Tech. J. 46, 1055 (1967) [7] J. Robertson, JAP, 100, 014111 (2006) [8] R. Callec et. al., JAP, 73, p. 4831. [9] C. H. Lee et. al., IEDM 09, p. 457

Strengths

- μ_h = 800-950 cm²/Vs
- μ_e =8-77×10⁴ cm²/Vs
- High CBO & VBO with lattice matched $Al_xGa_{1-x}Sb$
- Low temp processing

Challenges

- Highly reactive
- Need Good Dielectric
- Need Good Diode
- No MOSFET process
- Little process literature

Fig. 1: Strengths & challenges in development of a Sb based MOSFET

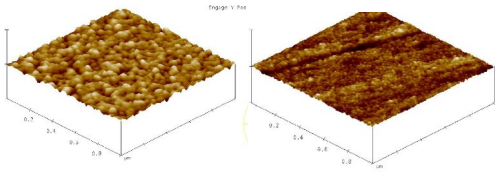

Fig. 2: Tapping mode AFM image of a GaSb left exposed in air for a long time shows (left) RMS roughness =4.014nm; after HCl Clean + 10 cycles ALD (right) RMS =0.727nm

Table. 1 : Surface roughness (nm) comparison

(100)	GaSb	Si	Ge
Pre Clean	0.355-4.014	0.28 [9]	0.15 [9]
After oxide	0.727	0.4 [9]	0.1 [9]

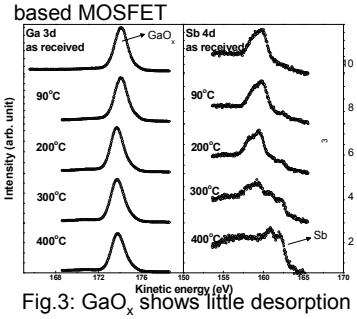

Fig.3: GaO_x shows little desorption till 400ºC during anneal under vacuum.

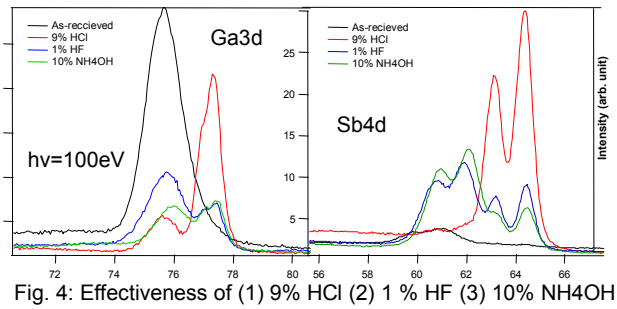

Fig. 4: Effectiveness of (1) 9% HCl (2) 1 % HF (3) 10% NH4OH clean in removing GaO_x & SbO_x is studied using SRPES

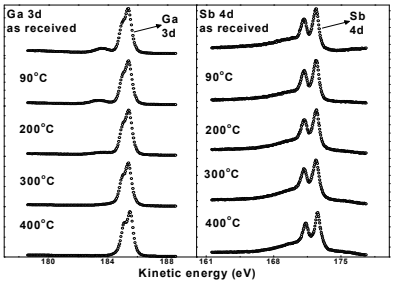

Fig. 5:Cleaning in HCl followed by annealing till 400ºC renders a surface free of native oxides.

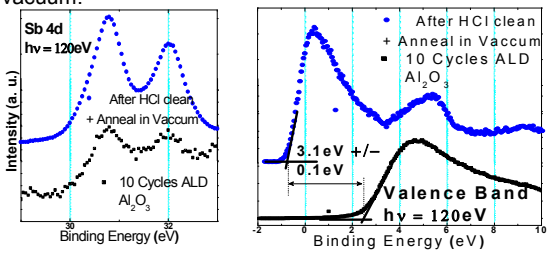

Fig. 6:VBO of Al_2O_3 on GaSb is calculated taking the difference in the valence band spectrum (right) Sb 4d peak from the substrate (left) is used for alignment.

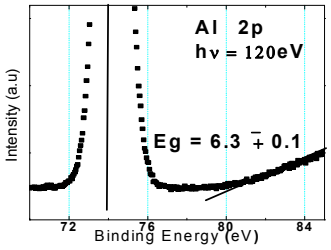

Fig. 7 : Bandgap is calculated from the Al 2p loss spectrum [4].

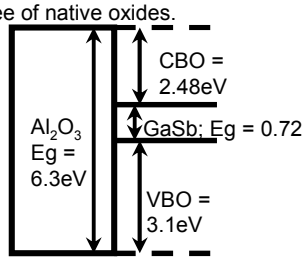

Fig. 8 : Band diagram for Al_2O_3 on GaSb.

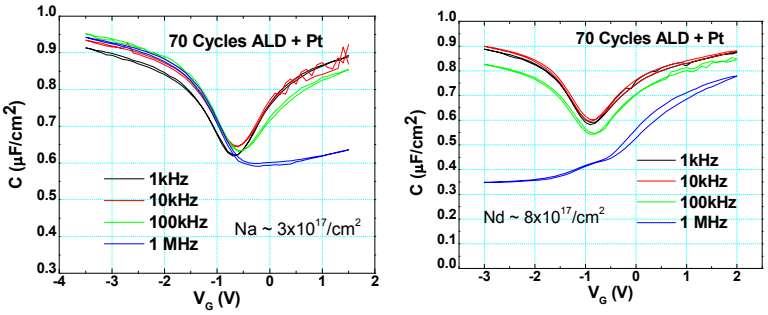

Fig. 9 : Measured CV's from 1kHz-1MHZ on p-type (left) & n-type (right) GaSb at 300K.

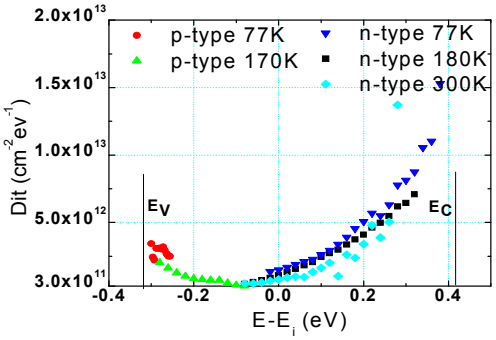

Fig. 10 : Dit distribution is calculated across the bandgap using conductance method. Mid bandgap Dit of 3×10¹¹ cm^{-2} eV^{-1} is achieved.

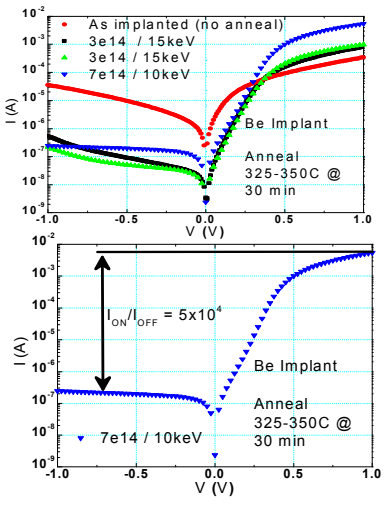

Fig. 11: Optimization of diode using different implant conditions (top) I_{ON}/I_{OFF} of 5X10⁴ was achieved (bottom)

- Field Oxide deposition
  Active area etch
- HCl Clean + 100 cyl.
  ALD Al_2O_3 @ 300ºC
- Al Gate patterning
- Be implant+ S/D liftoff
- 350ºC FGA anneal

Fig. 12: Process Flow

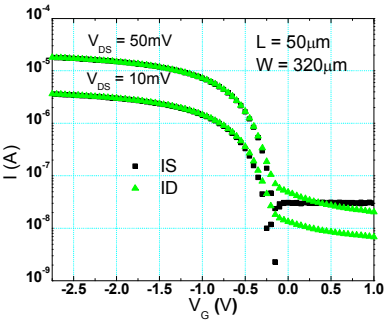

Fig. 13: I_D-V_G characteristics on the fabricated transistor.

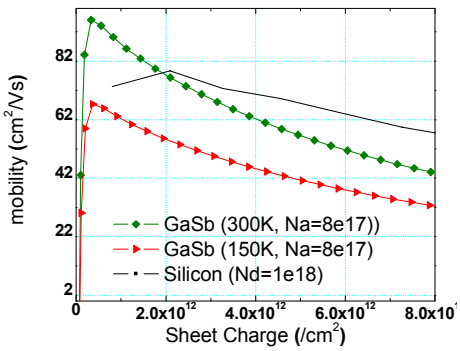

Fig. 14: Hole mobility vs. sheet charge at 300K and 150K calculated from the I_D-V_G @ 10meV & C_{GC} measured from the split CV measured.