A sub 350°C GaSb pMOSFET with ALD high-k dielectric

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Opportunity & Challenge: Sb based III-V semiconductors are one of the most promising device candidates for future high-speed, low-power logic applications. Some of the key strengths (Fig. 1) of Sb based semiconductors include: highest hole & electron mobility [1-2] among all III-V semiconductors, high conduction & valence band offsets (CBO/VBO) with lattice matched AlₓGa₁₋ₓSb for a heterostructure MOSFET design [1] and low thermal budget for MOSFET fabrication (as discussed later). The challenges in implementation of Sb based channels for CMOS is the highly reactive Sb surface (Fig. 2). A high quality dielectric and a good diode is needed for realization of Sb-MOSFETs. In this paper we attempt to overcome these challenges and fabricate a GaSb pMOSFET. GaSb is selected as it has the highest hole mobility amongst all III-Vs & has a bandgap of 0.72eV similar to Ge. pMOSFET was attempted first as it has been an implement in implementation of III-V complimentary logic.

Introduction: In this paper Synchrotron Radiation Photoemission Spectroscopy (SRPES) is used to study the effect of various chemical cleans & subsequent anneal in UHV on GaSb to render a surface free of elemental oxide & suitable for dielectric deposition. Bandgap & offsets for ALD AlₓOᵧ on GaSb are calculated using SRPES. Interface properties of the dielectric are investigated by analyzing the capacitance & conductance characteristics. A p/n diode on GaSb with I_on/I_off > 5×10⁶ is developed. Finally, output characteristics on a gate-first self-aligned GaSb pMOSFET are presented.

Surface/SRPES analysis: Desorption of SbOₓ and GaOₓ on as received GaSb was studied by annealing under UHV till 400°C. SbOₓ starts to desorb at 400°C and a Sb 4d peak from the substrate is observed, while GaOₓ is found to be thermally stable and no desorption till 400°C is observed (Fig. 3). Effectiveness of different chemical cleans on removing the GaOₓ and SbOₓ was studied low energy (hv=100eV) radiation from the synchrotron which allows observing the top few monolayers of the surface with great accuracy (Fig. 4). HF, HCl (acidic) and NH₄OH (basic) cleans were tried. While all HF, HCl & NH₄OH reduce GaOₓ, only HCl based clean is able to effectively reduce SbOₓ. A subsequent anneal after HCl clean reveals a GaSb surface free of native oxide (Fig. 5). Tapping mode AFM was used to study the surface, the RMS roughness just after HCl clean and after 10 cycles of ALD deposition were found to be 0.664 & 0.727nm respectively. Table 1 compares the RMS roughness with Si/Ge. As SRPES has a high energy resolution at the valence band spectrum maximum, VBO can be precisely extracted by taking difference between spectrum before/after AlₓOᵧ deposition (Fig. 6). VBO for AlₓOᵧ on GaSb was determined to be 3.1eV, Sb 4d peak from the substrate was used for alignment [4]. The Bandgap was determined to be 6.3eV from the Al 2p loss spectrum (Fig. 7) [4] which agrees well with values reported in literature for AlₓOᵧ deposited using ALD under similar conditions [5]. Taking the bandgap of GaSb (0.72eV) into account the band diagram was constructed as shown in Fig. 8. The CBO/VBO of 2.48eV/3.1eV for AlₓOᵧ on GaSb is sufficient to minimize the electron/hole tunneling and is suitable for MOSFET fabrication.

Process Development: Two key steps in developing a process for GaSb were the dielectric development for the gate stack and the source/drain junction formation.

(a) Dielectric: Fig. 9 shows the CV characteristics on capacitors made on n-type & p-type substrate. 70 cycles of ALD AlₓOᵧ were deposited at 300°C & Pt was used as the gate electrode. Inversion response was observed on both n/p-type GaSb. Frequency dispersion in accumulation is ~2%/decade for p-type & ~5%/decade for n-type. Higher frequency dispersion under accumulation in n-type GaSb suggests a higher Dit near the conduction band edge. Dit is calculated applying the conductance method (Fig. 10) in depletion region [6]. Both n/p-type substrates substrate are used for conductance measurement and the temperature is varied from 300K-77K to probe the Dit distribution across the entire bandgap. A mid bandgap Dit of 3×10¹¹ cm⁻² eV⁻¹ is obtained. The Dit distribution is asymmetric with an order of magnitude higher Dit towards the conduction band side, this is in qualitative agreement with the fact that CNL of GaSb is located at ~0.1eV from the valence band edge [7].

(b) Diode Development: Obtaining good diode characteristics in GaSb using ion implantation has been a problem traditionally, due to hillock formation because of implant damage [8]. Zn & Be which act as shallow acceptors in GaSb were tried for formation of p/n diode. Hillock formation was observed with Zn (dose 3×10¹⁴/cm²) which couldn’t be removed by annealing in RTA. Only Be (being a lighter atom) implant was successful with high enough dose suitable for transistor fabrication. Fig. 11 shows the diode characteristics with various implant conditions. Sheet resistance decrease with anneal temperature saturates at 350°C and good diode characteristics with I_on/I_off of >5×10⁶ with ideality factor of 1.3 could be obtained with annealing at 350°C for 30 min (Fig. 11). There is room for further improvement with more optimization of implant dose and energy.

Process Flow: The low temperature required for S/D activation allows for a gate-first process flow. Fig. 12 summarizes the process flow : 100 cycles (~10nm) of ALD AlₓOᵧ deposited at 300°C was used as the gate dielectric followed by Al evaporation and gate patterning. S/D contacts were formed with Ti/Ni liftoff, Fabrication of the transistors was completed with a 350°C FGA anneal which also activates the S/D implant. Maximum temperature during the entire process flow never exceeds 350°C.

Transistor Results: Fig. 13 plots the I₉/V₉ for GaSb pMOSFET. I_on/I_off of >10⁴ was obtained. Mobility vs. sheet charge in Fig. 14 is extracted on using I₉/V₉ on the L₉=100μm device at V_DS=10mV & sheet charge is calculated from the Cᵥ measurements at 100kHz. No corrections for S/D resistance are applied. Hole mobility in our device is comparable to silicon with similar doping density. Mobility in our device decreases with decrease in temperature (Fig. 14) indicating the mobility is not limited by phonon scattering mechanisms. Mobility in the high sheet range could be limited by the interface roughness which was measured to be 3-4 times higher in GaSb as compared to Si/Ge (Table 1).

Summary: ALD AlₓOᵧ gate stack & p/n diode are developed on GaSb. Peak inversion hole mobility of 85cm²/Vs is the highest reported to date for GaSb pMOSFET.

Table 1: Surface roughness (nm) comparison

<table>
<thead>
<tr>
<th>Condition</th>
<th>GaSb</th>
<th>Si</th>
<th>Ge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre Clean</td>
<td>0.355</td>
<td>0.28</td>
<td>0.15</td>
</tr>
<tr>
<td>After HCl clean</td>
<td>0.727</td>
<td>0.4</td>
<td>0.1</td>
</tr>
</tbody>
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Fig. 2: Tapping mode AFM image of a GaSb left exposed in air for a long time shows (left) RMS roughness ≈ 4.014nm; after HCl Clean + 10 cycles ALD (right) RMS ≈ 0.727nm

Fig. 3: GaO₃ shows little desorption till 400°C during anneal under vacuum.

Fig. 4: Effectiveness of (1) 9% HCl (2) 1% HF (3) 10% NH4OH clean in removing GaO₃ & SbO₃ is studied using SRPES

Fig. 5: Cleaning in HCl followed by annealing till 400°C renders a surface free of native oxides.

Fig. 6: VBO of Al₂O₃ on GaSb is calculated taking the difference in the valence band spectrum (right) Sb 4d peak from the substrate (left) is used for alignment.

Fig. 7: Bandgap is calculated from the Al 2p loss spectrum [4].

Fig. 8: Band diagram for Al₂O₃ on GaSb.

Fig. 9: Measured CV’s from 1kHz-1MHZ on p-type (left) & n-type (right) GaSb at 300K.

- Field Oxide deposition
- Active area etch
- HCl Clean + 100 cyl.
- ALD Al₂O₃ @ 300°C
- Al Gate patterning
- Be implant + S/D liftoff
- 350°C FGA anneal

Fig. 10: Dit distribution is calculated across the bandgap using conductance method. Mid bandgap Dit of 3x10¹¹ cm⁻² eV⁻¹ is achieved.

Fig. 11: Optimization of diode using different implant conditions (top) Iₓ₀/Vₓₓ of 5x10⁻² was achieved (bottom).

Fig. 12: Process Flow

Fig. 13: Iₓ₀/Vₒ characteristics on the fabricated transistor.

Fig. 14: Hole mobility vs. sheet charge at 300K and 150K calculated from the Iₓ₀-Vₒ @ 10meV & Cₒc measured from the split CV measured.