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Integration Technologies for GaN Power Transistors

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1. Introduction

AlGaN/GaN hetero-junction transistors (HFETs) are very promising for power switching applications taking advantages of the high breakdown strength together with the inherent high carrier density owing to the unique polarization induced charges. The device has a lateral configuration, of which the low on-state resistance makes it very compact. It can be easily integrated onto one chip, while conventional Si-based power transistors with the vertical device configuration are very difficult to be integrated. The GaN devices are thus advantageous for monolithic integration of power switching circuits. The integration can reduce the size and cost of the systems as well as it can reduce the operating loss by eliminating the parasitic components.

In this paper, newly developed technologies for monolithic integration of GaN power switching transistors are reviewed. The topics include the world first GaN-based inverter IC, a novel chip layout eliminating undesired surface flashover to achieve high breakdown voltages with low on-state resistances.

2. Monolithic Integration of GaN Inverters

Monolithic integration of GaN transistors requires high enough breakdown voltages between the devices to enable their independent control. The device isolation also needs to be thermally stable typically over 800°C since it needs to be compatible with the high temperature processing of the GaN transistors. Here, Fe ion implantation successfully forms the planar isolation regions onto AlGaN/GaN, which maintains high resistivity over 800°C. The Fe ion forms deep levels by its substitution of the Ga site in GaN after full recovery of the processing damage by the ion implantation. Fig.1 shows a schematic cross section of a part of the fabricated GaN monolithic inverter IC for motor drive. Six normally-off AlGaN/GaN Gate Injection Transistors (GITs) are integrated on a cost-effective Si substrate, between which the isolation regions are formed by Fe ion implantation [1,2]. The specific on-state resistance and the off-state breakdown voltage of the GIT on Si are 2.0mΩcm^2 and 700V, respectively. The isolation region serves the breakdown voltage of 900V after the annealing at 1200°C as shown in Fig.2. The chip photograph and the circuit diagram of the fabricated inverter IC is shown in Fig.3 This GaN inverter IC successfully drives a motor with high efficiency taking advantages of the low on-state resistance and low switching loss. Fig.4 shows the resultant operating efficiency as a function of the output power of the motor. The results for an inverter consisted of discrete Si-IGBTs (Insu lated Gate Bipolar Transistors) are also plotted. The operating loss is 42% reduced in the fabricated GaN inverter IC from that in conventional IGBT-based one.

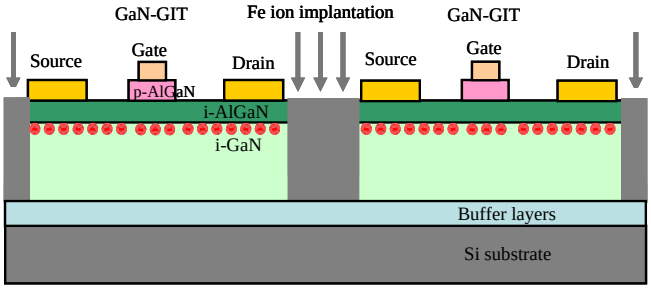

Fig.1 Schematic cross secion of a part of the GaN-based inverter IC using isolation regions by Fe ion implantation over GITs on a Si substrate.

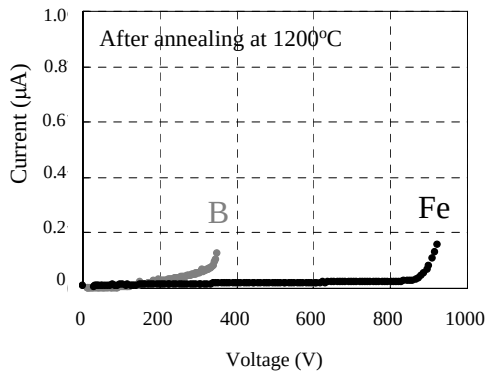

Fig.2 Isolation characteristics between 5μm spacing of the Fe and B ion-implanted isolation regions after annealing at 1200°C.

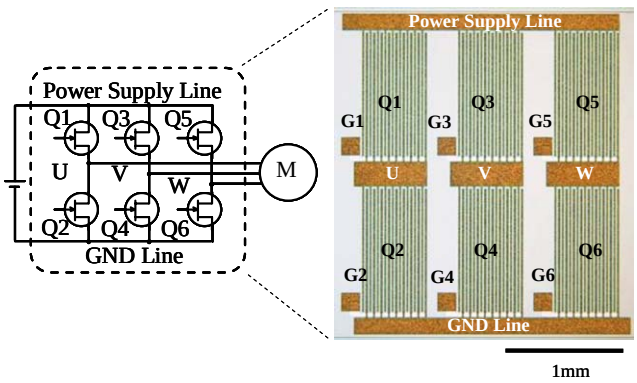

Fig.3 Chip photograph with a circuit diagram of fabricated GaN monolithic inverter IC.

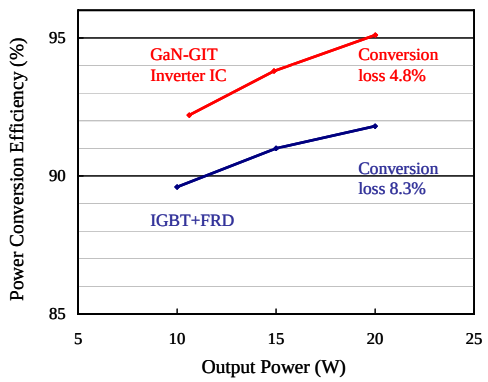

Fig.4 Power conversion efficiency of GaN monolithic inverter and that by conventional Si-IGBTs with FRDs(Fast recovery diodes) at various output power of the motor.

3. Efficient Chip Layout of GaN Trnasistors Using Via-holes

GaN power switching transistors have lateral device configurations which require more area for the source/drain electrodes on the top surface than that by vertical devices. To minimize the area of such surface electrodes and to reduce the chip cost and size of the discrete GaN power device, use of a backside electrode connected to the surface electrodes through via-holes is demonstrated. The device structure with source via-holes relieves the electric field since the employed conductive Si substrate underneath the GaN device acts as a backside field plate [3]. The one with drain via-holes with closely packed chip layout with poly-AlN passivation with high breakdown strength eliminates undesired surface flashover between the surface electrodes by eliminating the crossover of them, resulting in extremely high breakdown voltages over 10kV[4,5]. The cross sectional structure of the latter device and the chip photograph are shown in Fig.5 and Fig.6, respectively. The via-holes through chemically stable sapphire substrates are formed by newly developed laser drilling technique using a high power short-pulsed laser. The use of the AlN passivation and minimizing the area of the drain electrodes on the surface successfully eliminates the surface flashover. The resultant maximum off-state breakdown voltage of the AlGaN/GaN HFET is as high as 10400V by the extension of the gate-drain spacing as shown in Fig.7. The value is the highest ever reported for GaN-based transistors.

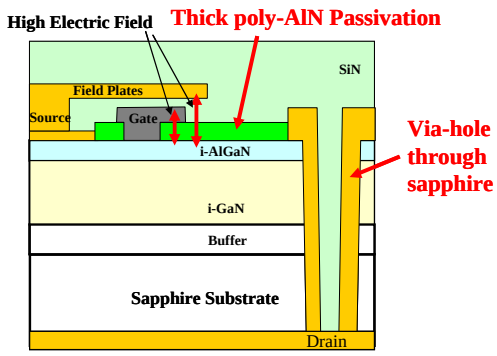

Fig.5 Schemetic cross-section of the fabricated ultra high voltage AlGaN/GaN HFETs with AlN passivation and via-holes through sapphire substrate.

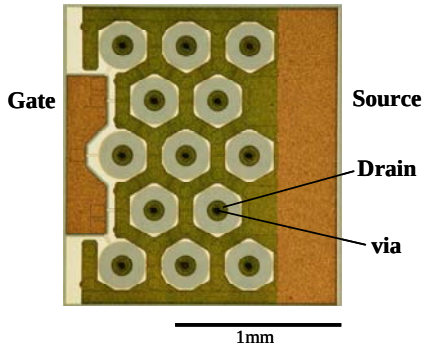

Fig.6 Chip photograph of the fabricated ultra high voltage AlGaN/GaN HFET array.

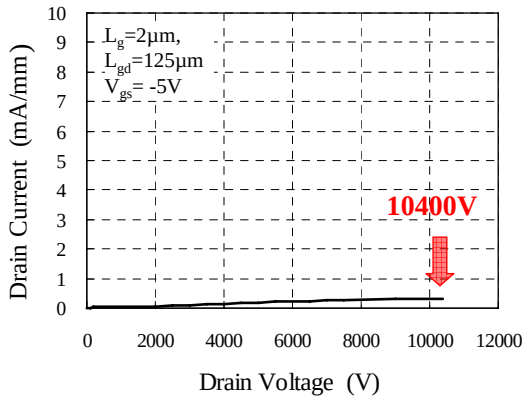

Fig.7 Off-state Ids-Vds characteristics of the fabricated high voltage AlGaN/GaN HFET.

4. Conclusions

Novel integration technologies for GaN power switching transistors are reviewed. Use of Fe ion implantation for the device isolation serves high breakdown voltages of 900V between the isolation regions which enables the world first GaN-based inverter IC for motor drive. Integration of via-holes for a backside electrode with very efficient chip layout is also presented, which achieves high breakdown voltages over 10kV. These technologies are indispensable for wide-spread use of GaN transistors in the future.

Acknowledgments

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References

[1] Y. Uemoto et al., IEEE Trans. Electron Device, **54** (2007) 3393.
[2] Y.Uemoto et al., IEDM2009 Tech. Dig. (2009) 165.
[3] M. Hikita et al., IEEE Trans. Electron Device, **52** (2005) 1963.
[4] Y. Uemoto et al., IEDM2007 Tech. Dig. (2007) 861.
[5] N. Tsurumi et al., IEEE Trans. Electron Device, **57** (2010) 980.